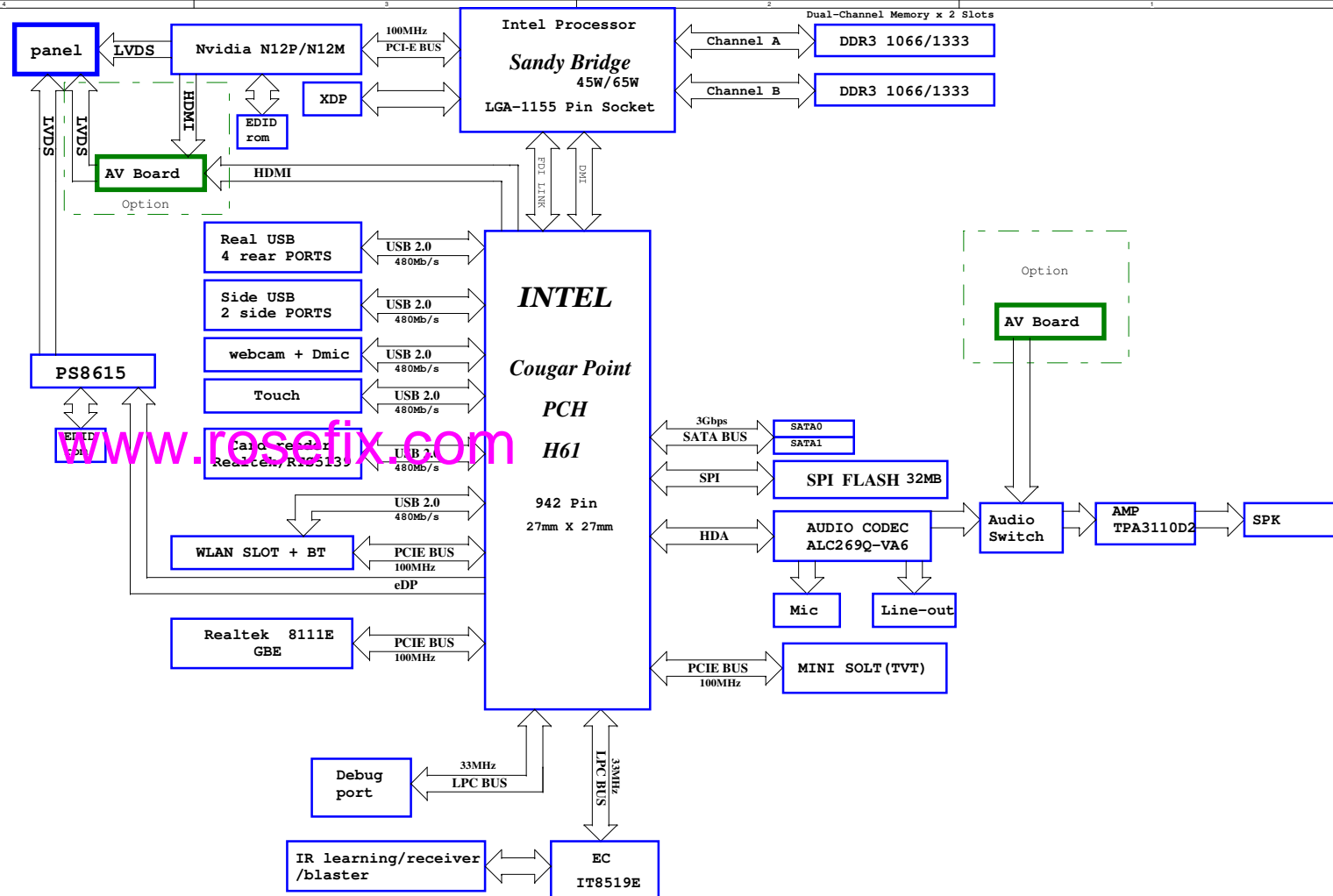
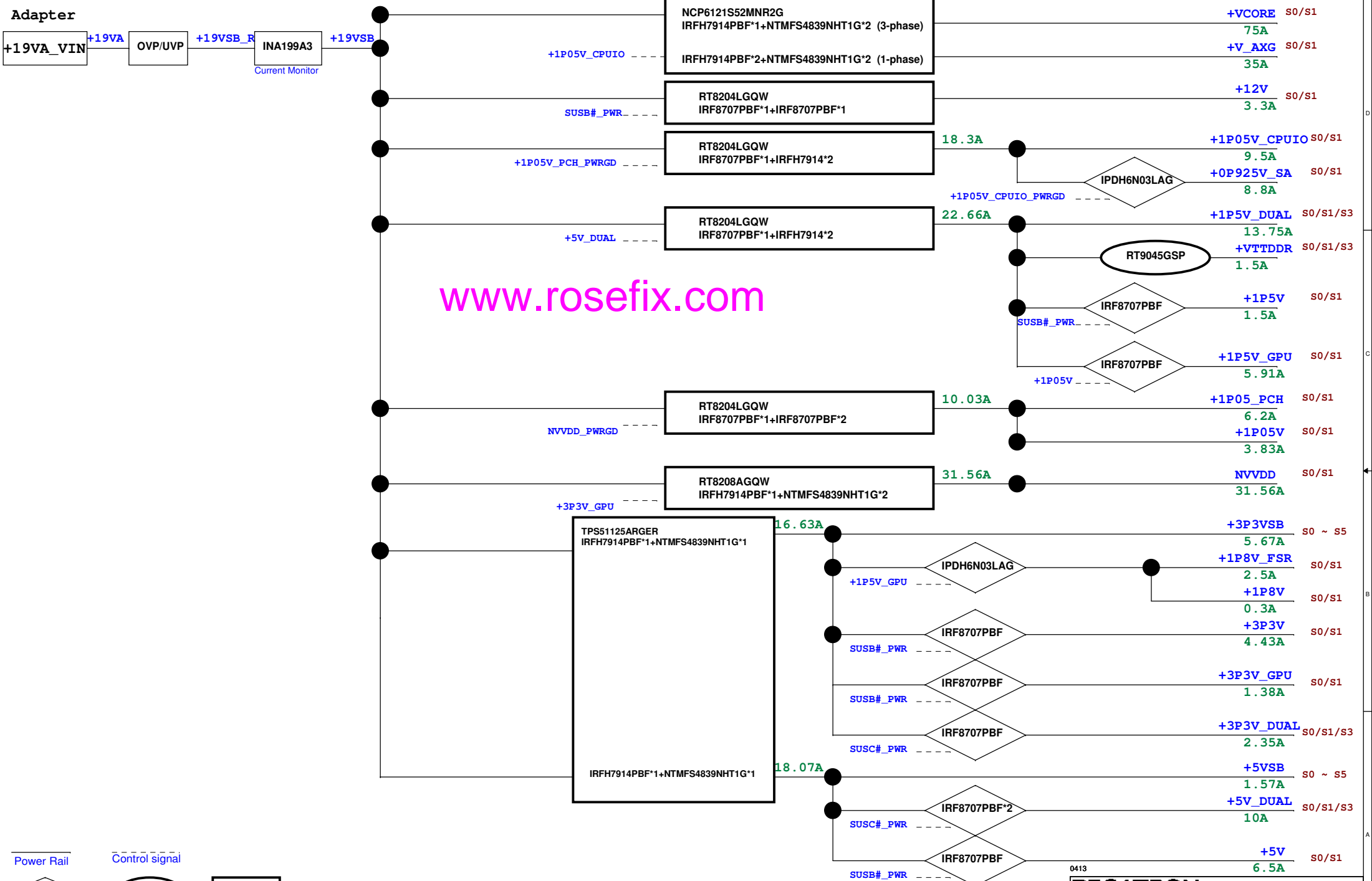


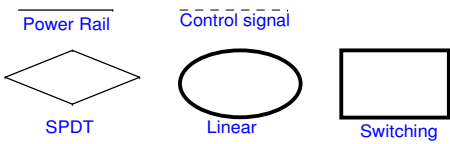
IPPSB-FA

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01	BLOCK DIAGRAM
02	POWER FLOW
03	POWER SEQUENCE
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10	DDR3 CHANNEL A G/F
11	DDR3 CHANNEL B G/F
12	DDR3 TERMINATION A&B
13	PLTRST CPU# + Smbus
14	Converter Controller
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27~28	LAN
29~30	CODEC&CONN
31~32	AMP&SWITCH
33~35	USB&HUB&BT
36	HPD_DET
37~38	MINI_CARD(WL&TVT&DMC)
39	Misc. conn&Touch&Wcam&RTC
40	FAN
41	PWR_LED + Button*
42	IR_LEDS
43~44	EC 8519
45	SM_BUS + SPI_ROM
46	SCREW_HOLE
47	UVP, OVP + +19VSB
48	LOAD_SWITCH
49	+3P3VSB&+5VSB
50	+1P5V_DUAL + +1P2V
51	Current Monitor
52	+12V + +1P8V
53	+1P05V_CPUIO&+0P925V_SA
54	POWER_PROTECT
55	+1P05V_CPUIO_CAP
56	+VTT_DDR
57	+V_AXG_DRIVER
58	+VCORE_CONTROLLER
59~61	+VCORE_CAP
62	+1P05V&+1P05V_PCH
63~64	CPU&PCH_XDP_DEBUG_CONNECTOR
65	VGA_CONN
66~67	GPU_DDR3
68	VGA-N12P_STRAPPING+EEPROM
69	MXM.VGA-N12P_Xtal/Thermal
70~71	GPU_HDMI(DMC&AV)
72	GPU_CTRL
73	GPU.VGA_N12P_PCI-E I/F
74	GPU_PCI-E_LVDS_VGA
75	MXM.GPU_Discharge
76	GPU_POWER&GND
77	MXM.NVDD
78	Card Reader RTS5139-GR
79	EDP_CH7511





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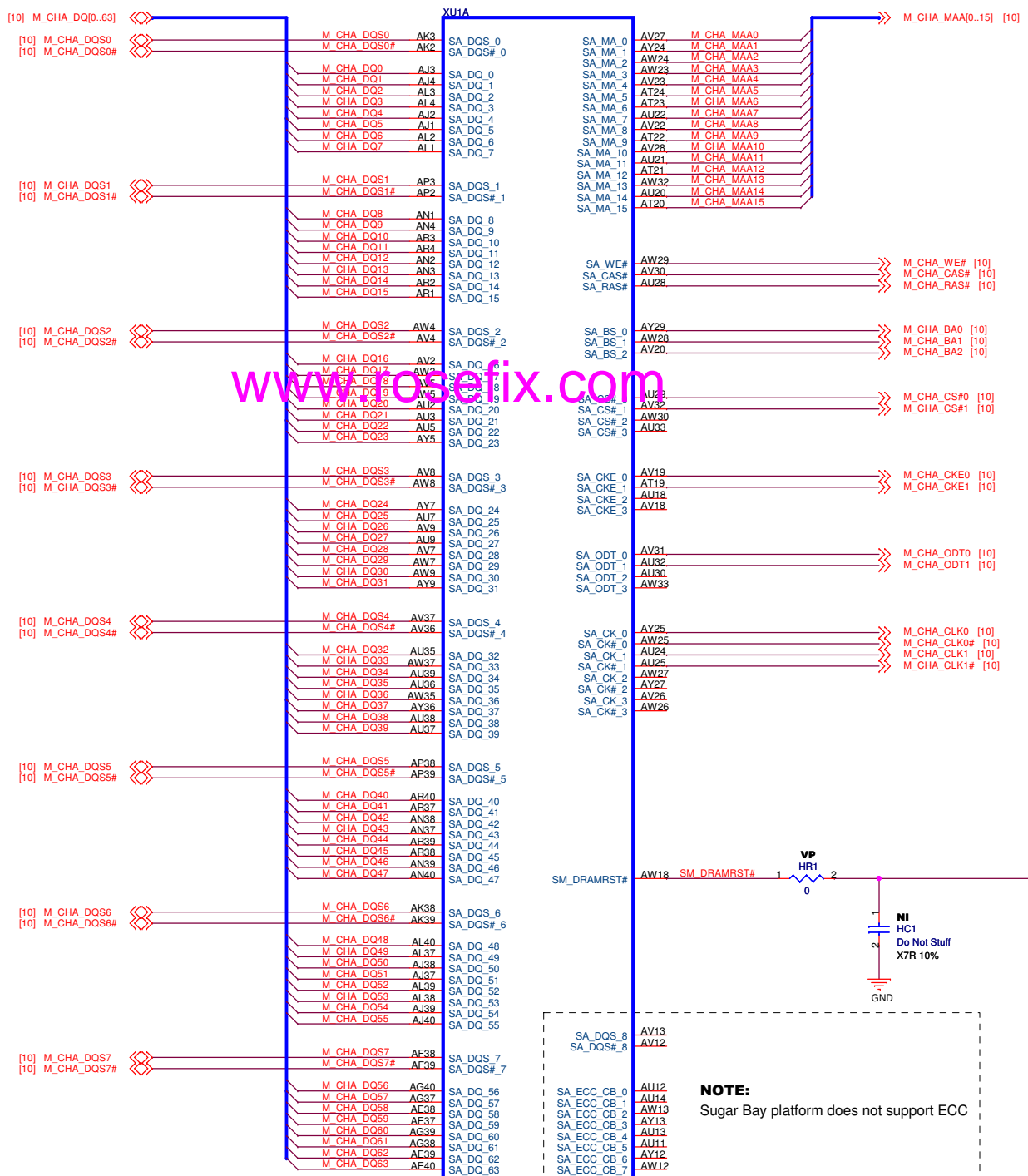
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PEGATRON Title : POWER FLOW

PEGATRON CORPORATION Engineer: XXXX-XX

Size A3	Project Name IPPSB-FA	Rev 1.01
Date: Tuesday, April 26, 2011		Sheet 2 of 79



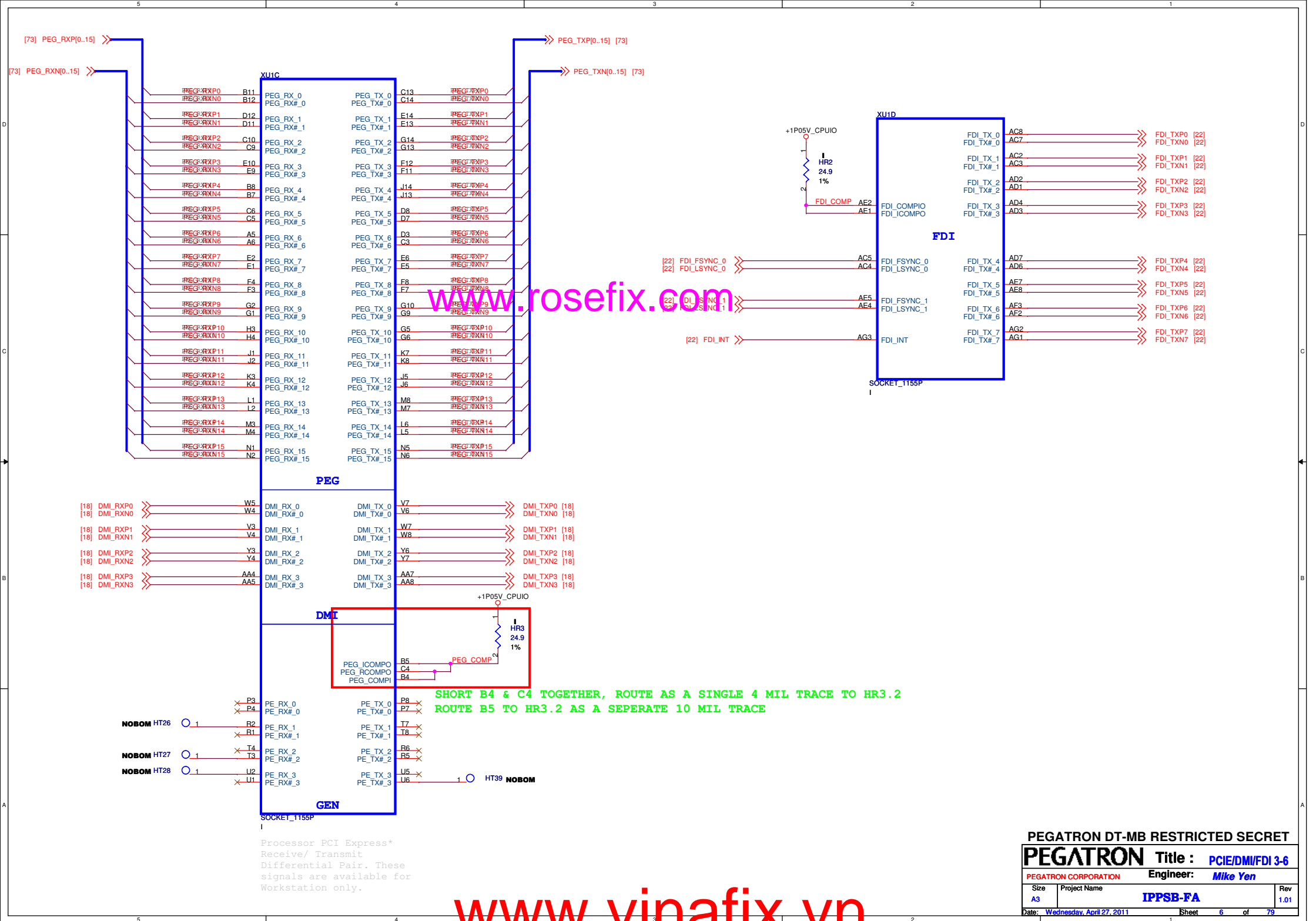
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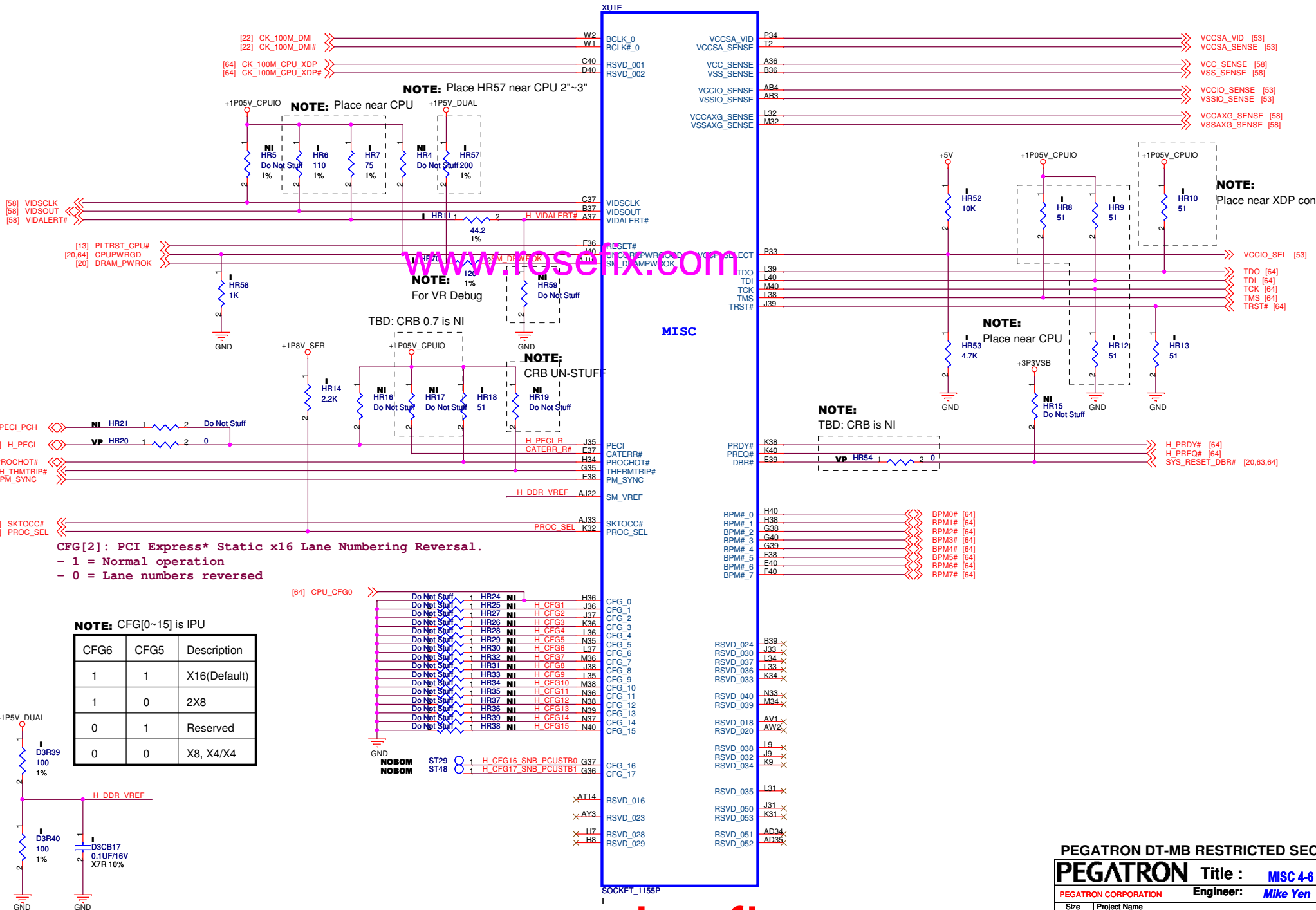
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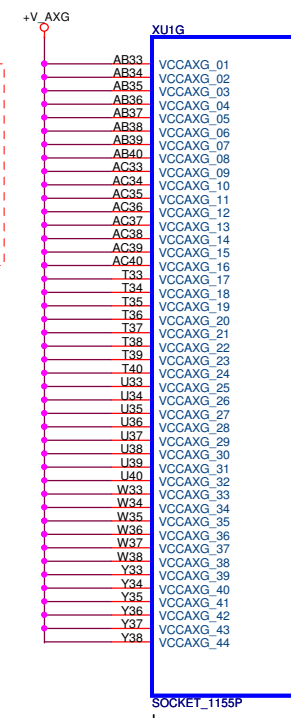
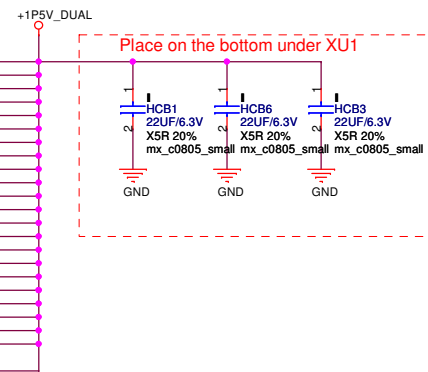
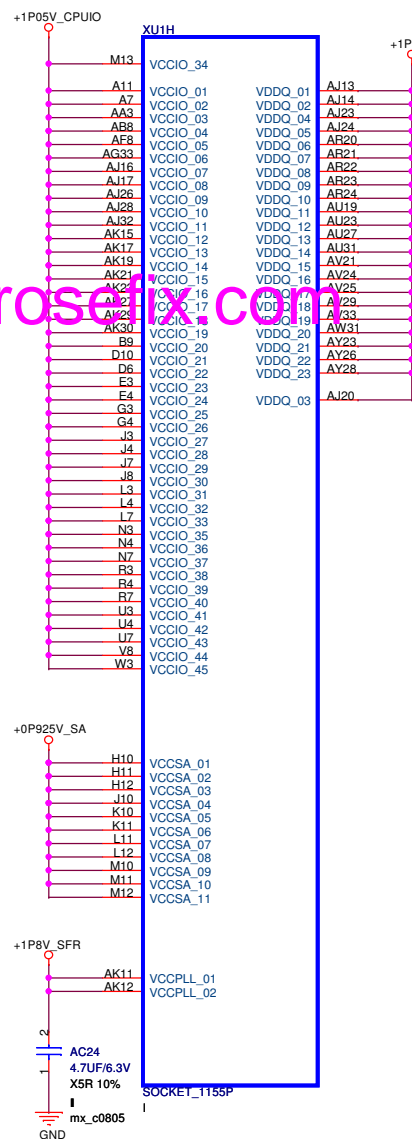
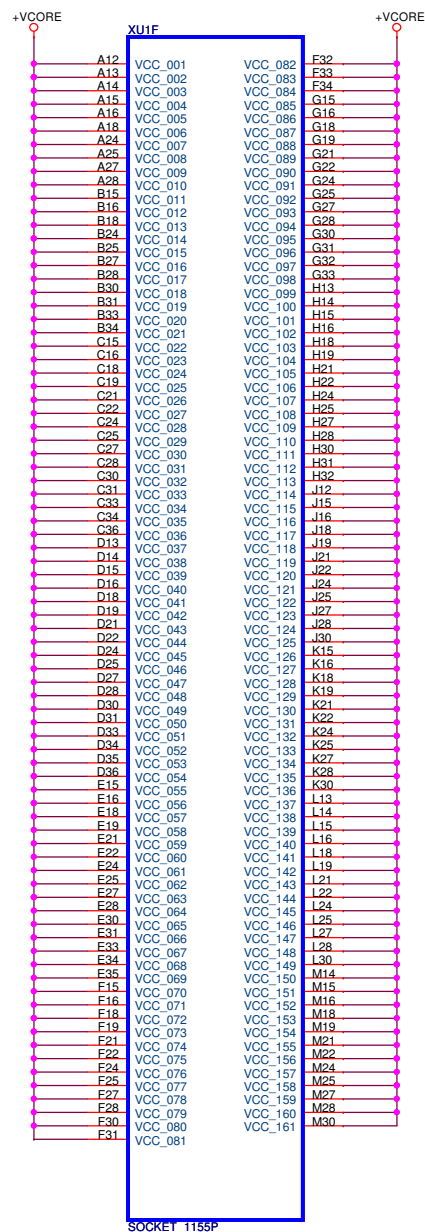
PEGATRON CORPORATION Engineer: **Mike Yen**

Size A3	Project Name IPPSB-FA	Rev 1.01
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PEGATRON DT-MB RESTRICTED SECRET

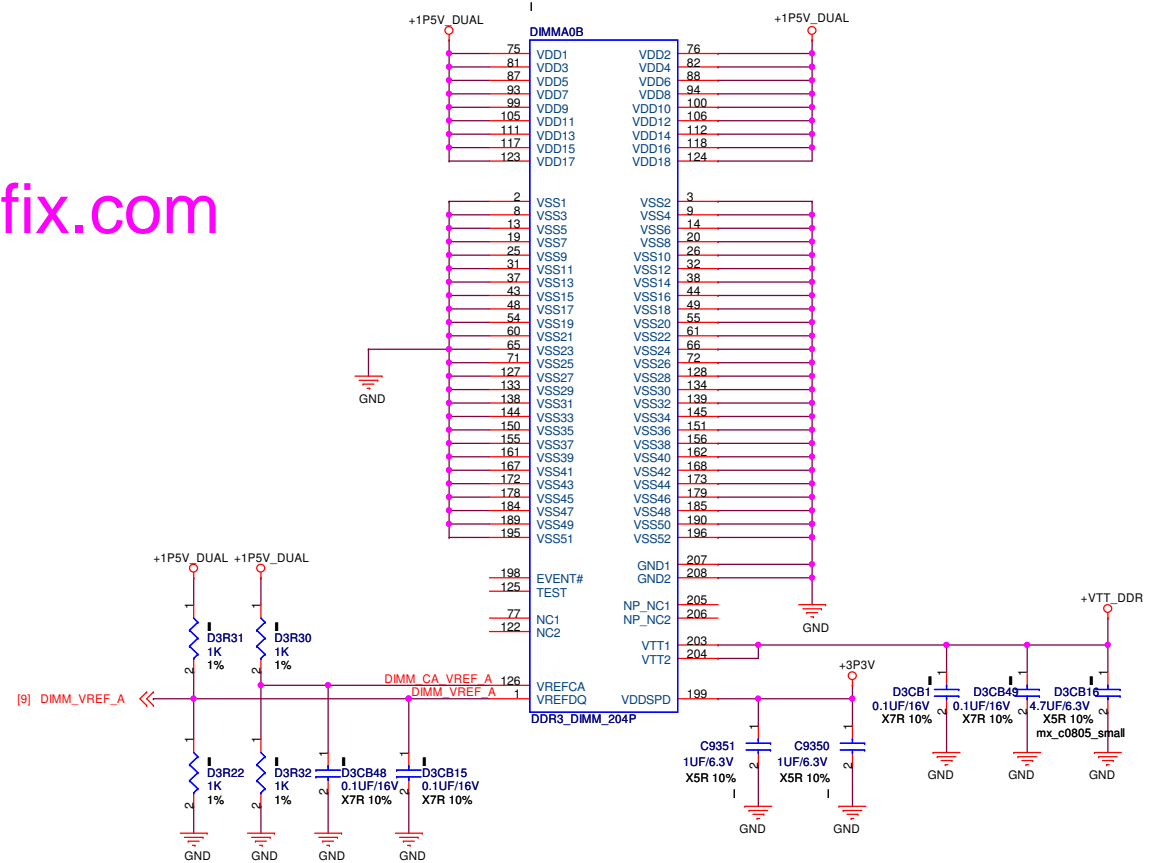
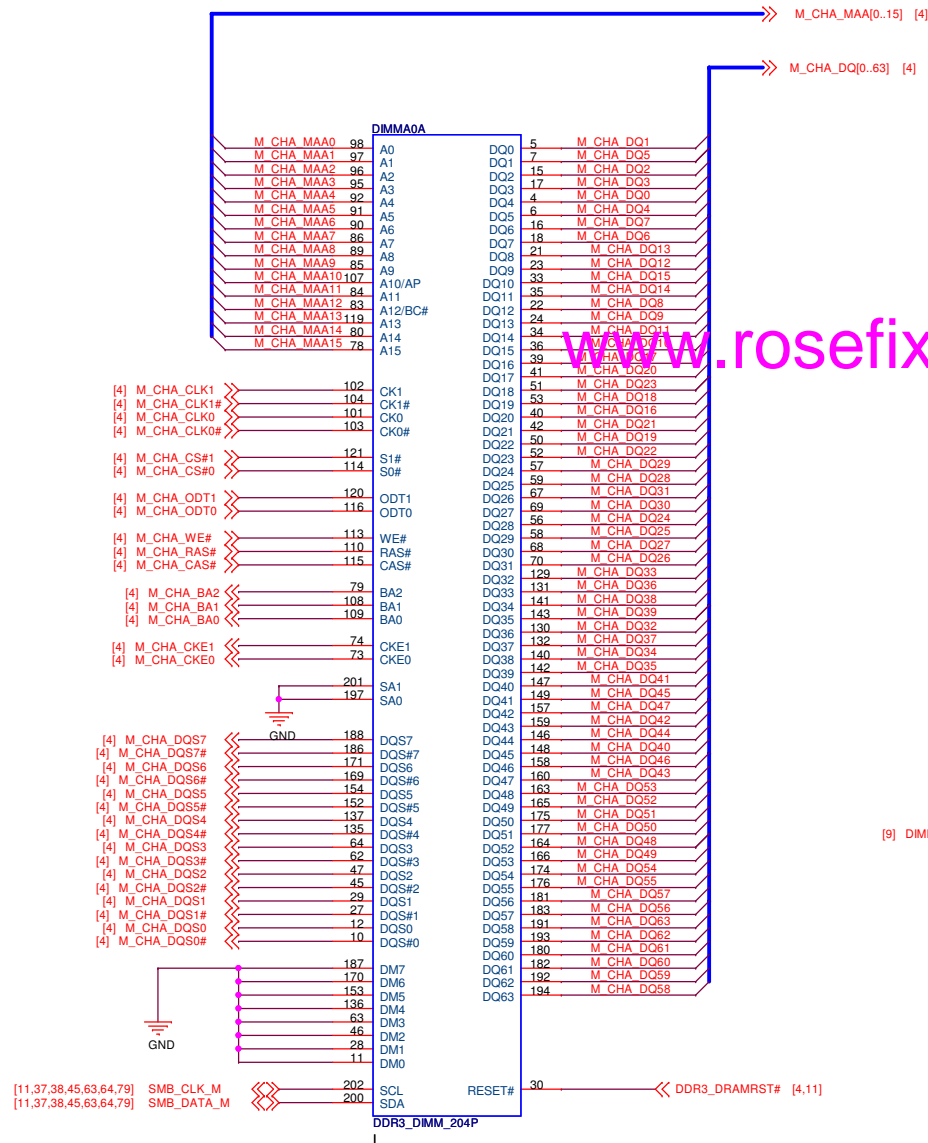
PEGATRON Title : VCC 5-6

PEGATRON CORPORATION Engineer: Mike Yen

Size A3 Project Name IPPSB-FA Rev 1.01

Date: Tuesday, April 26, 2011 Sheet 8 of 79

皆改爲5.2H

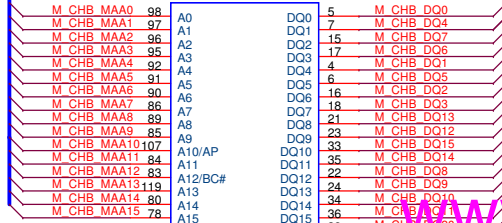


皆改爲5.2H

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M_CHB_MAA[0..15] [5]

(5.2H)
DIMMB0A



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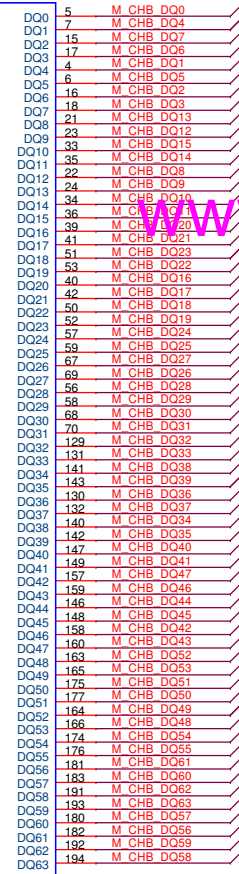
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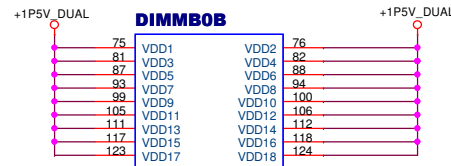
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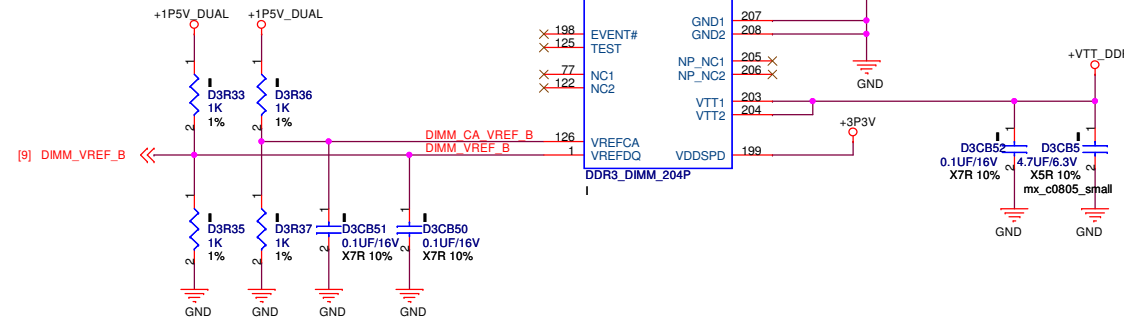


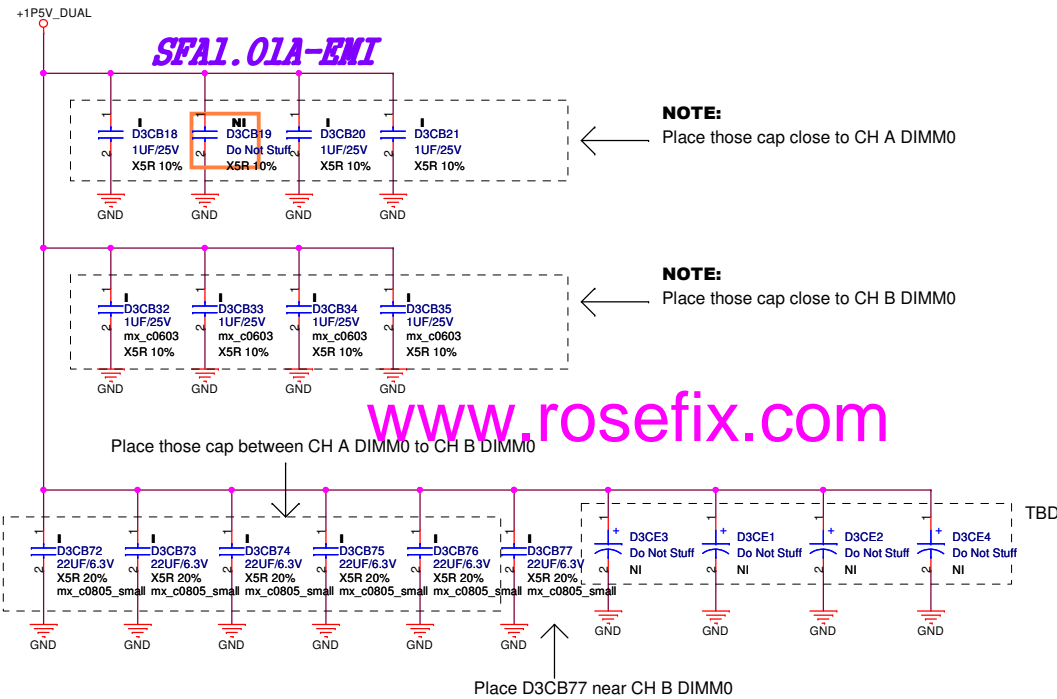
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GND

DIMMB0B



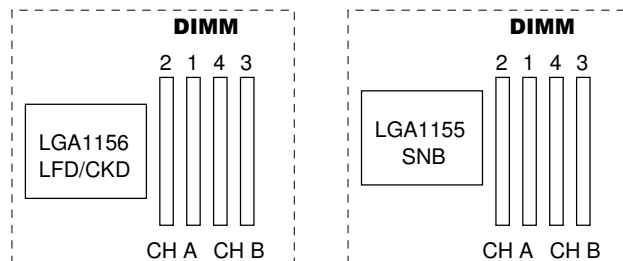
GND





NOTE:

DIMM Placement for different platform



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PEGATRON Title : DDR3 TERMINATION A&B

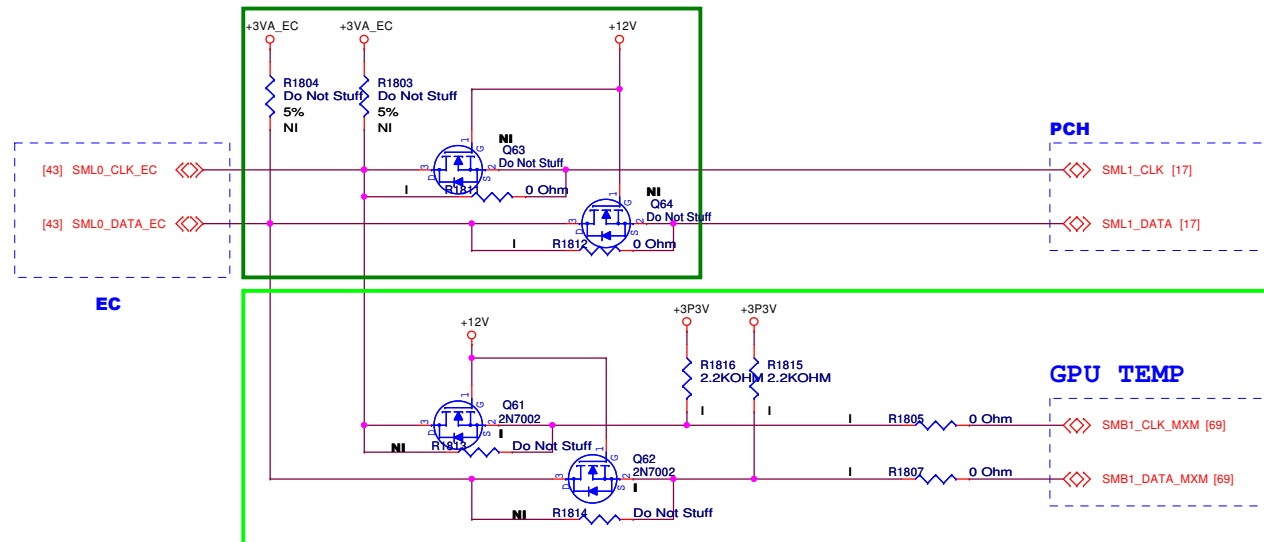
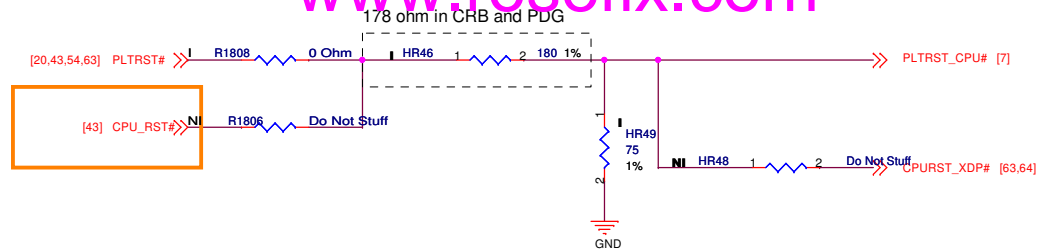
PEGATRON CORPORATION Engineer: Mike Yen

Size A3 Project Name IPPSB-FA Rev 1.01

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PLTRST_CPU#

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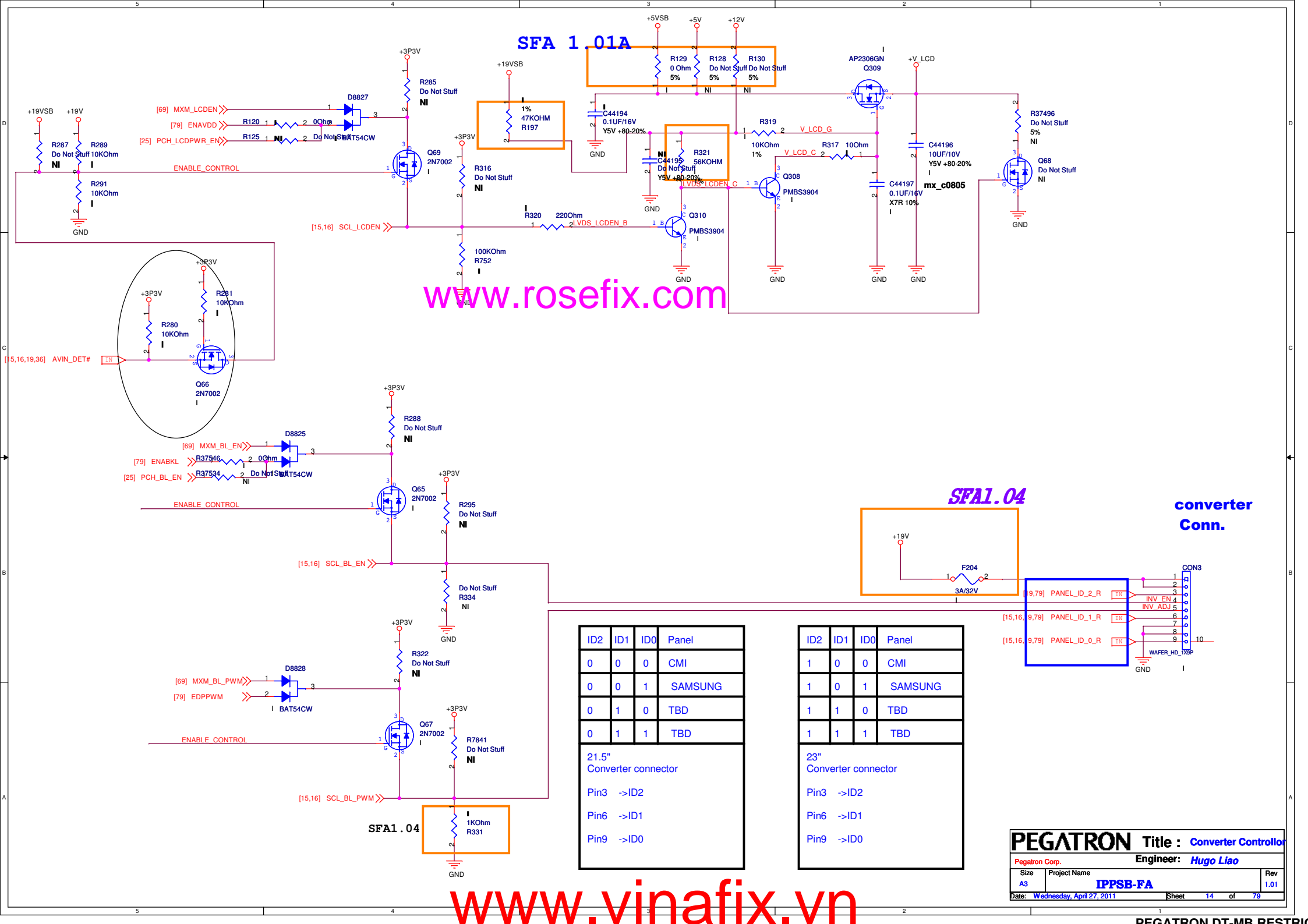
PEGATRON Title : PLTRST_CPU#&SMBus

PEGATRON CORPORATION Engineer: XXXX-XX

Size A3	Project Name IPPSB-FA	Rev 1.01
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SFA 1.01A

SFA1.04

converter Conn.

ID2	ID1	ID0	Panel
0	0	0	CMI
0	0	1	SAMSUNG
0	1	0	TBD
0	1	1	TBD

21.5"
Converter connector
Pin3 ->ID2
Pin6 ->ID1
Pin9 ->ID0

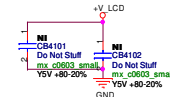
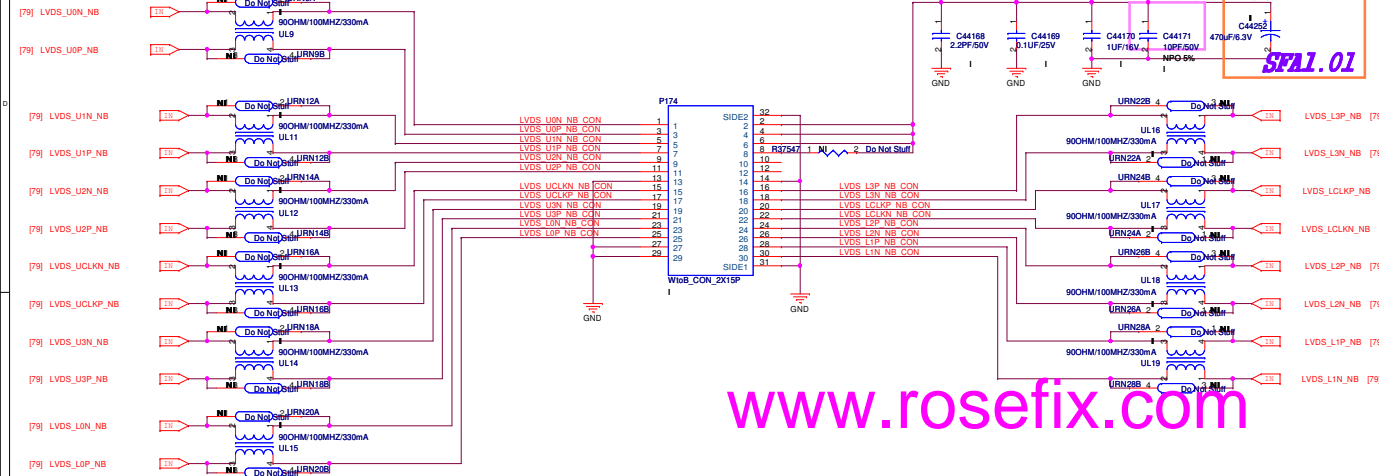
ID2	ID1	ID0	Panel
1	0	0	CMI
1	0	1	SAMSUNG
1	1	0	TBD
1	1	1	TBD

23"
Converter connector
Pin3 ->ID2
Pin6 ->ID1
Pin9 ->ID0

已修改完成

LCD CONN NB & GPU colay

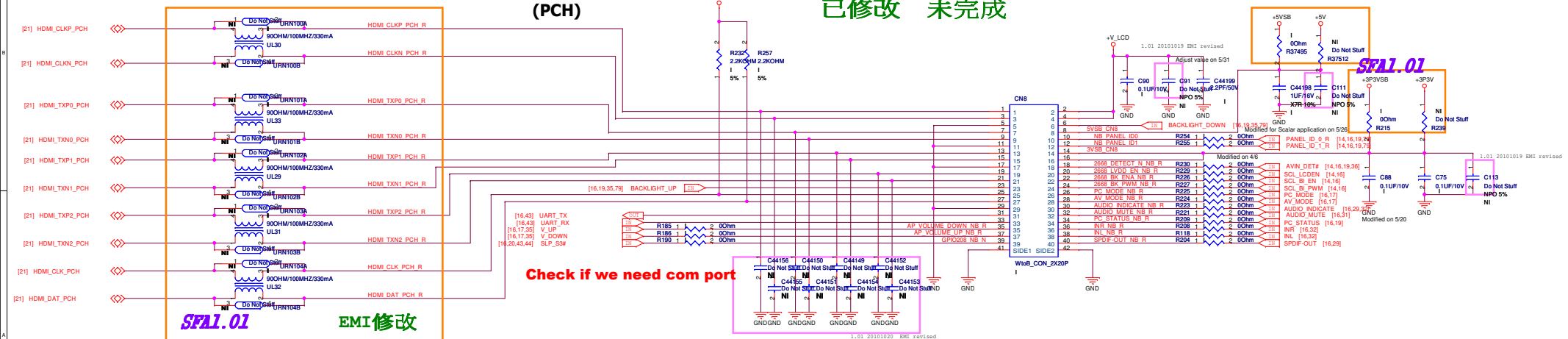
LVDS CONN (PCH)



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AV Board connector (PCH)

已修改 未完成



Check if we need com port

www.vinafix.vn

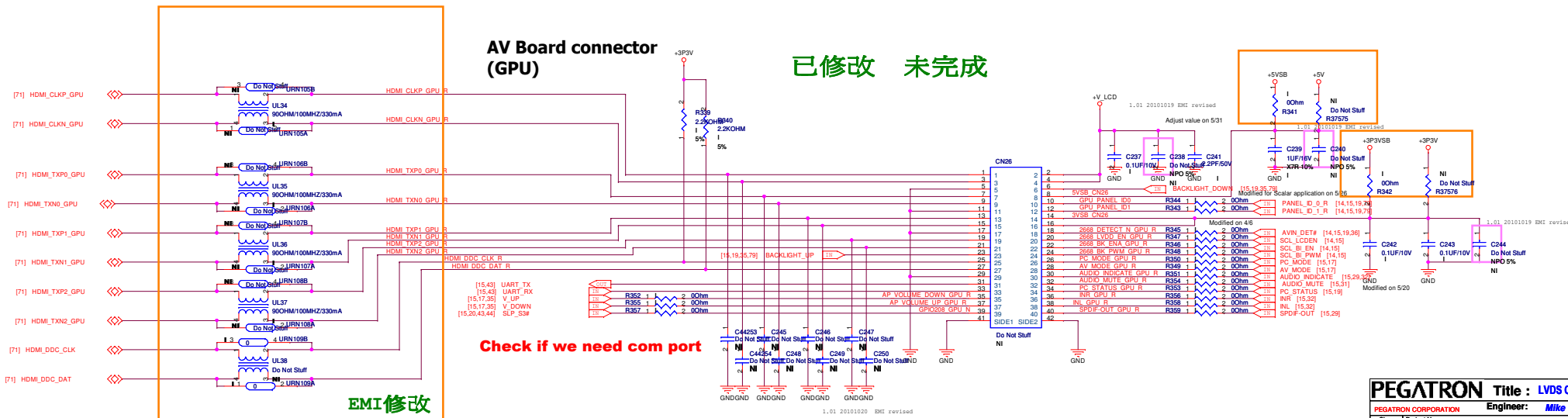
LVDS CONN (GPU)



SFA1.01

AV Board connector (GPU)

已修改 未完成



Check if we need com port

EMI修改

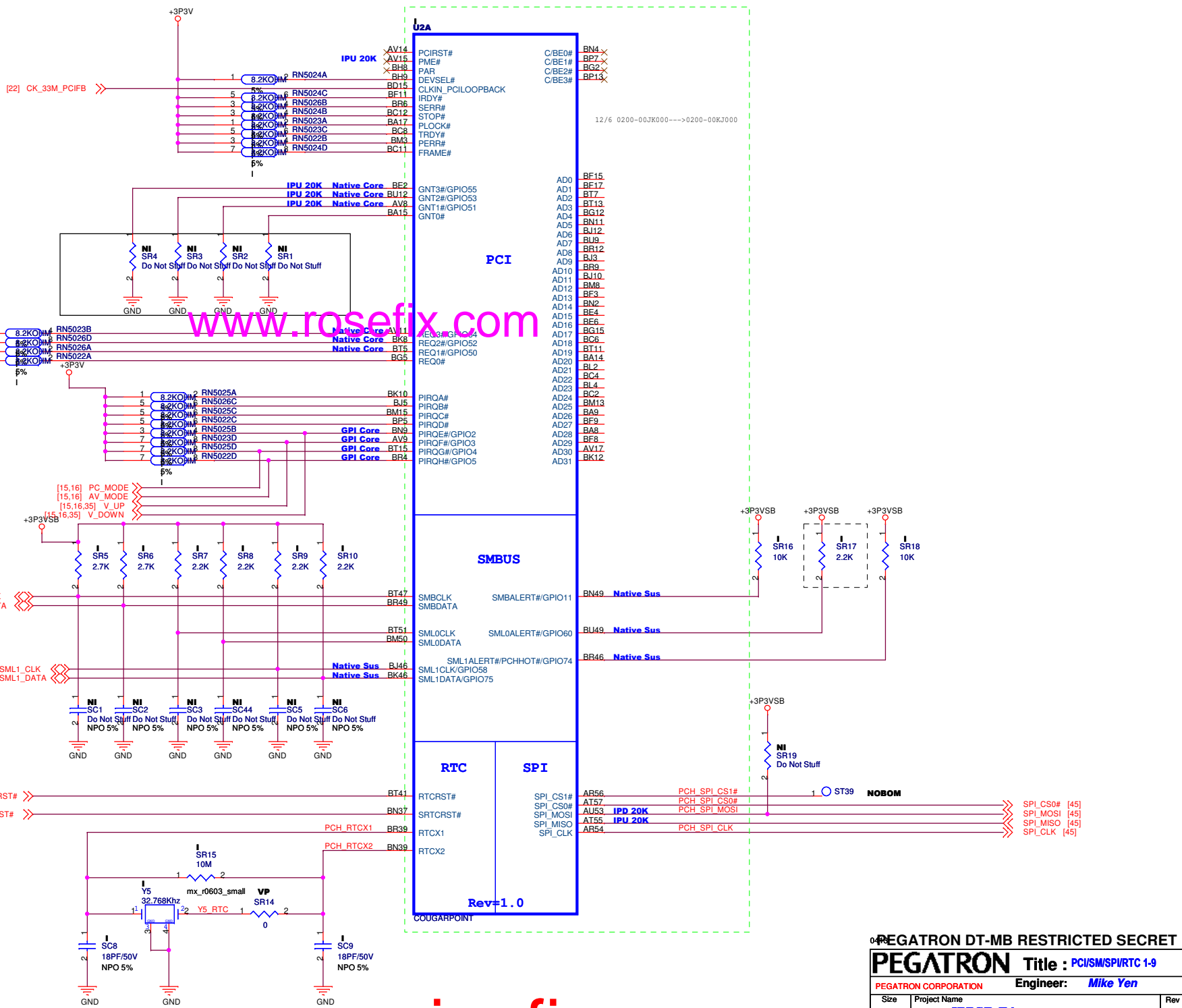
PEGATRON		Title : LVDS CON	
PEGATRON CORPORATION		Engineer: Mike Yen	
Size	Project Name		R
A2	IPPSB-FA		1/

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NOTE: Strapping Options Flash

GNT1#	SATA1GP /GPIO19	Boot Device
0	0	LPC
1	0	PCI
1	1	SPI

I2C/en(dis)able/S3
for accelerometer



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NOTE: HDA_SYNC
On-die PLL VR voltage selector.
Hi: supplied by 1.5V.
Low: supplied by 1.8V.

NOTE: HDA_SDO
Disable ME in Manufacturing mode
--> connect to 3.3VSB.

NOTE: CRB 0.7 is 1.1K ohm with 1%
For platform not supporting deep sleep connect directly to RSMRST#.
The DSW rails must be stable for at least 10 ms before DPWROK is asserted to PCH.

[13,43,54,63] PLTRST#
[7,63,64] SYS_RESET_DBR#

[43] PM_RSMRST#
[43,63] DPWROK

SLP_SUS#

LPC

LDRQ1#/GPIO23
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
IPU 20K BK15
IPU 20K BJ17
IPU 20K BJ20
IPU 20K BG20
IPU 20K BK17
BG17
FWH4/LFRAME#

AUDIO

HDA_SDO
HDA_SYNC
HDA_BCLK
HDA_RST#
JTAG_TMS
JTAG_TDO
JTAG_TDI
JTAG_TCK
TP12

BMBUSY#/GPIO0
CLKRUN#/GPIO32
HDA_DOCK_EN#/GPIO33
STP_PCI#/GPIO34
GPIO35
GPIO36
LAN_PHY_PWR_CTRL#/GPIO12
HDA_DOCK_RST#/GPIO13
GPIO15
GPIO24/MEM_LED
GPIO28
SLP_LAN#/GPIO29
GPIO27
GPIO31

PCIECLKRQ2#/GPIO20
PCIECLKRQ5#/GPIO44
PCIECLKRQ6#/GPIO45
PCIECLKRQ7#/GPIO46
GPIO57

NOTE:
SUSACK# and SUSWARN#
can be tied together if EC/SIO
does not want to involve in
the handshake mechanism
for the Deep Sleep state
entry and exit.

SLP_S3#
SLP_S4#
SLP_SS#/GPIO3
SLP_A#
SLP_SUS#

AW55 GPI Core
BC56 GPO Core
BC25 GPO Core
BL56 GPI Core
BJ57 GPO Core
BP51 GPO Sus IPU 20K
BK50 Native Sus
BA25 GPO Sus
BM55 GPO Sus IPU 20K
BP53 GPO Sus GPIO24 MEM_LED
BJ55 GPO Sus IPU 20K
BH49 GPO Sus
BJ43 GPI DSW IPU 20K
BG43 GPI DSW IPU 20K

AV43 Native Core
BL54 Native Sus IPU TBD
AV44 Native Sus IPU 20K
BP55 Native Sus IPU 20K
BT53 GPI Sus

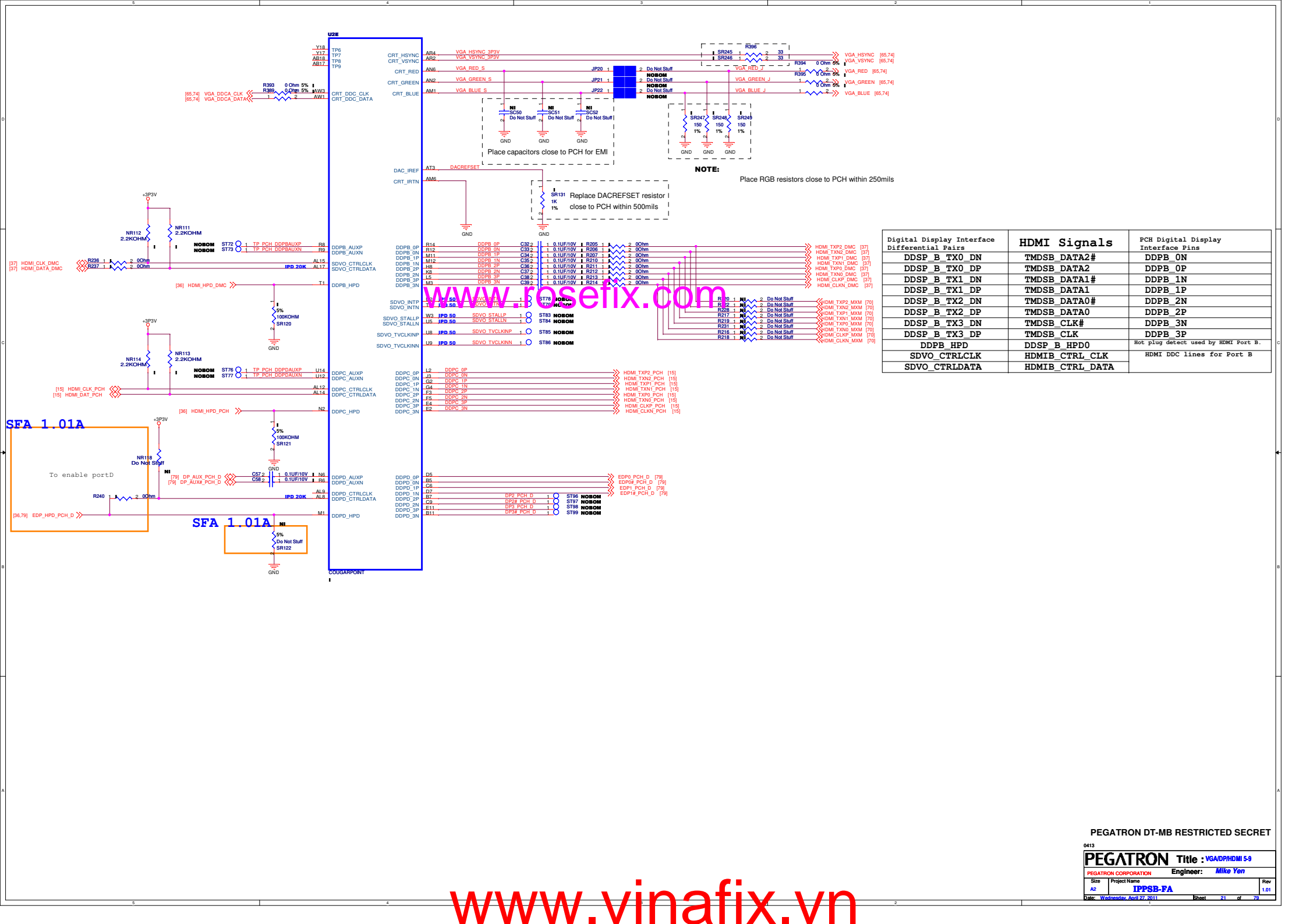
BATLOW#/GPIO72
SUSWARN#/SUSPWRDNACK/GPIO30
SUSACK#
SUSCLK#/GPIO62
SUS_STAT#/GPIO61

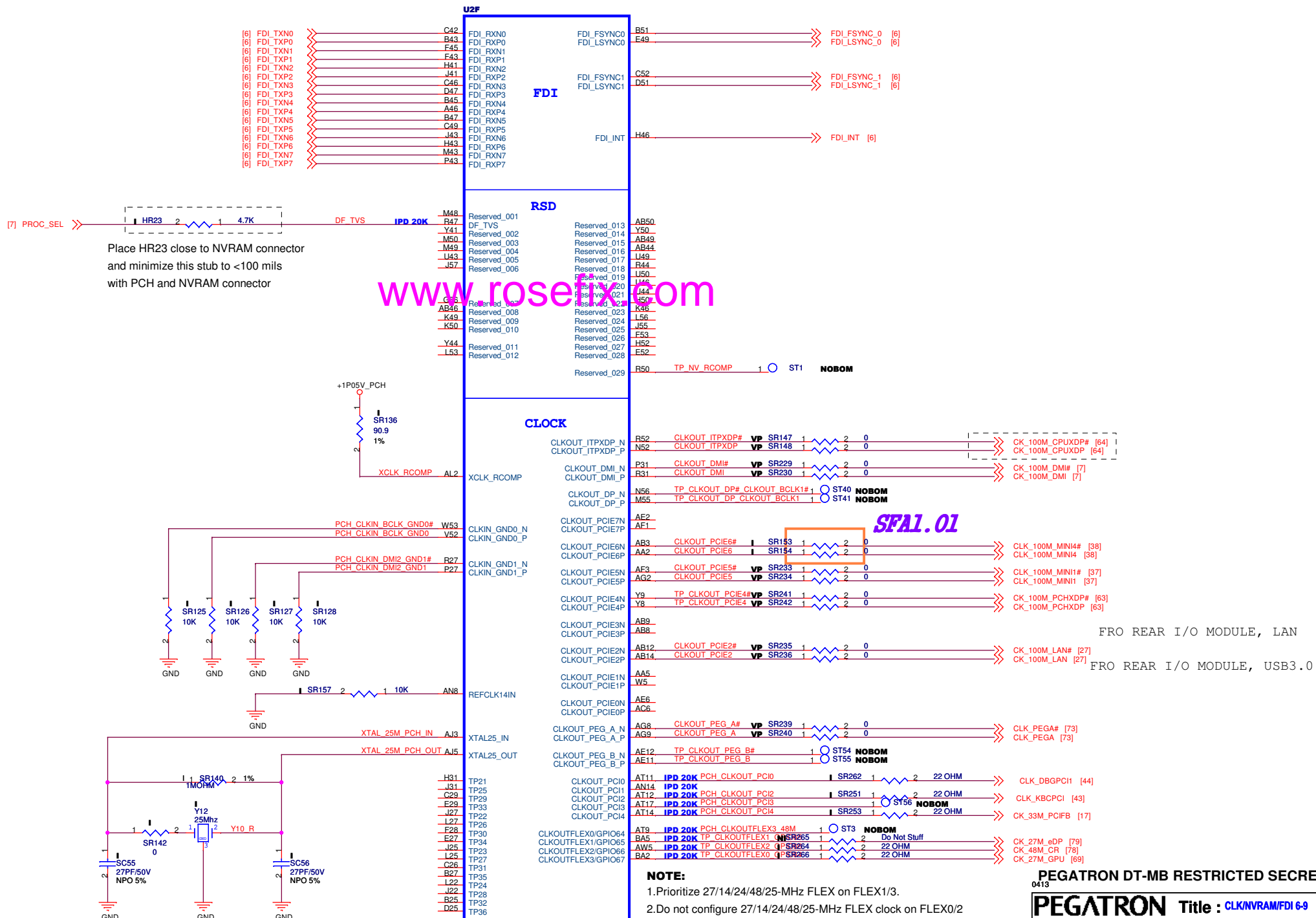
AV46 Native Sus IPU 20K
BU46 GPI DSW
BP45 IPU TBD
BA47 Native Sus
BN54 Native Sus

RI#
WAKE#
INTRUDER#
SPKR
PWRBTN#
BT43 IPU 20K
BM53
BN52
BL50
BC41
BD43

SLP_S3# [15,16,43,44]
SLP_S4# [43,44]
SLP_A#
SLP_SUS# [43]

PIN	HIGH	LOW	DESCRIPTION
GPIO15	Enable	Disable	TLS confidentiality
GPIO28	Enable	Disable	On-Die PLL VR





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SFA1.01

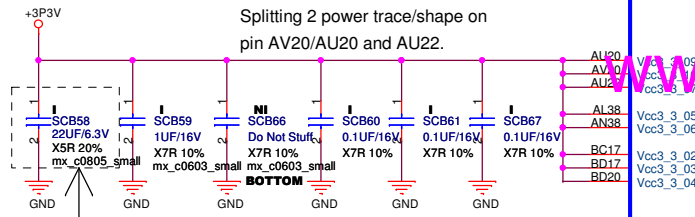
www.vinafix.vn

NOTE:

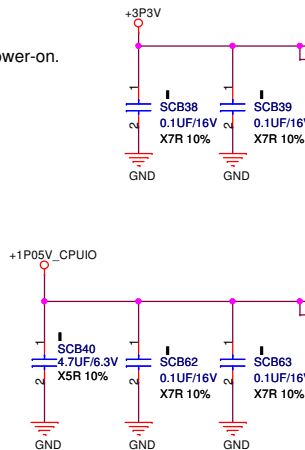
Place SCB59 and SCB66 near pin AU20,
SCB60 near pin AL38,
SCB61 and SCB67 near BC17.

NOTE:

Splitting 2 power trace/shape on
pin AV20/AU20 and AU22.

**NOTE:**

Install SCB58 during initial power-on.

**NOTE:**

Just for measurement.

CRB 0.7 is 1uF

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NOTE:

NI or install is decided to DSW support or not.

**NOTE:**

Install SCB31 during initial power-on.

NOTE:

Splitting 2 power trace/shape on
pin AV28, AY31/AY33, and AV30/AV32.

NOTE:

Place SCB53 near pin BT35, SCB54 near pin U31,
and SCB69 near pin AV30/AT40.

NOTE:

Place SCB56 near PCH within 40mils.

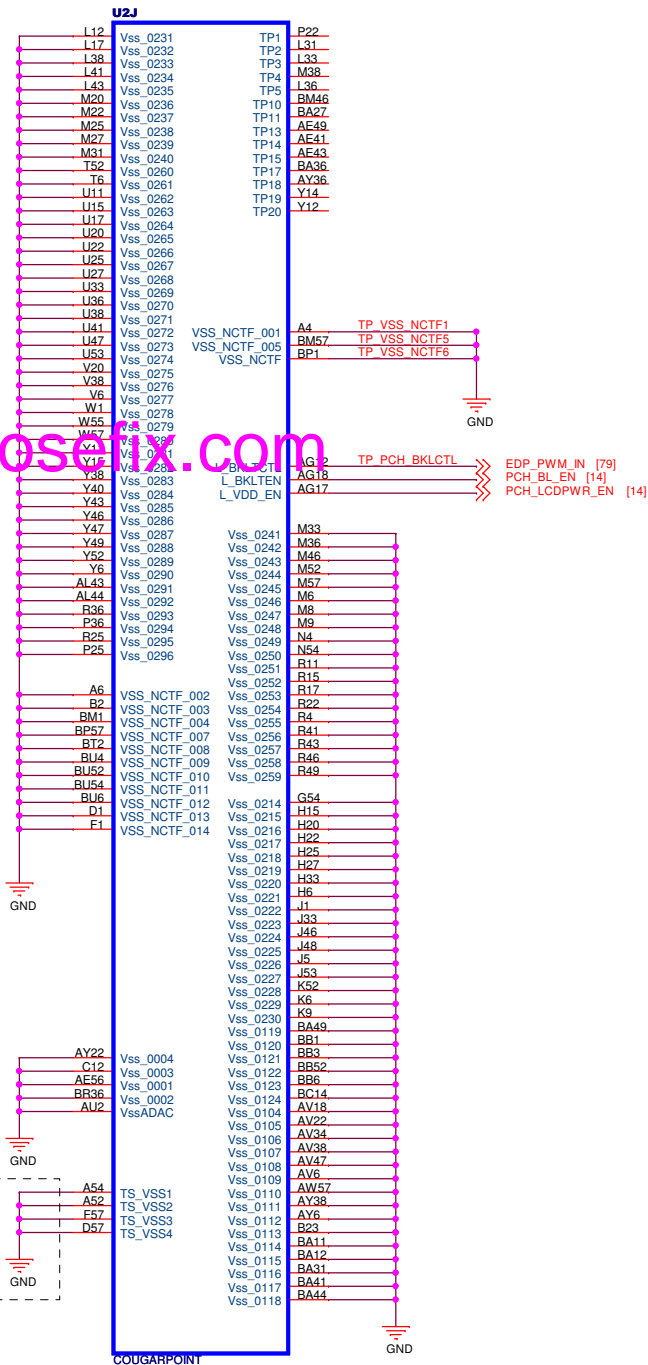
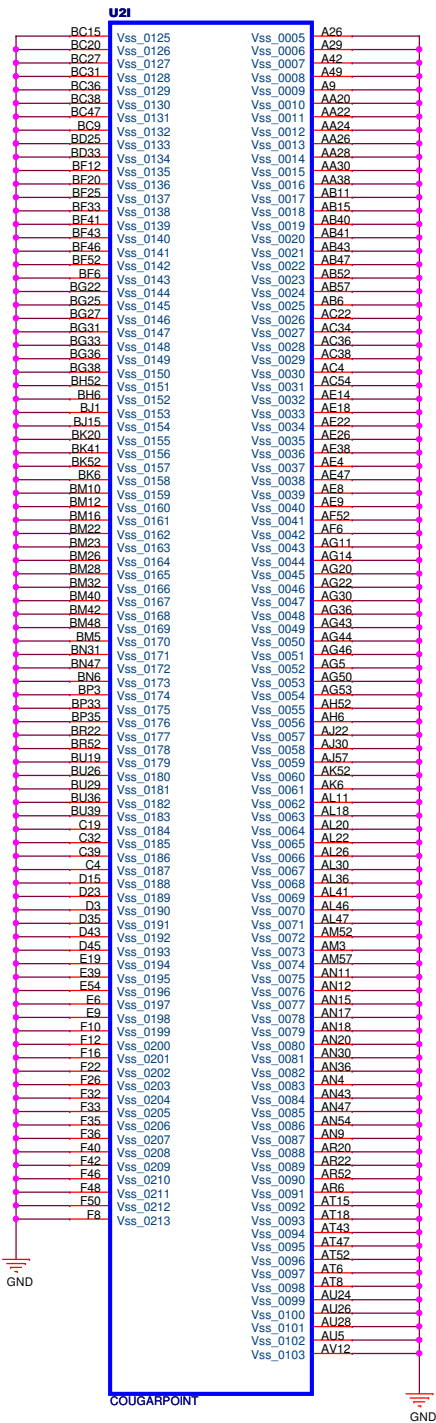
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VCCSUS 8-9

PEGATRON CORPORATION Engineer: Mike Yen

Size A3 Project Name IPPSB-FA

Date: Tuesday, April 26, 2011 Sheet 24 of 79



NOTE:
BOM option depend on thermal result

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PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VSS 9-9

PEGATRON CORPORATION Engineer: Mike Yen

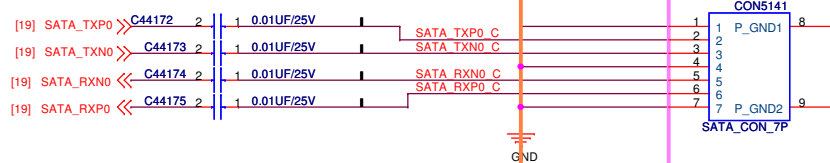
Size	Project Name	Rev
A3	IPPSB-FA	1.01

Date: Wednesday, April 27, 2011 Sheet 25 of 79

已更改完成

SATA HDD CON

1.01 20101019 revised



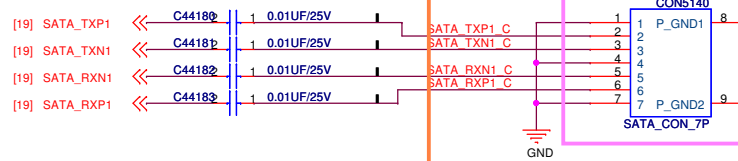
SATA CONTROLLER #1
(MASTER)

COLOR = DARK BLUE

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SATA ODD CON

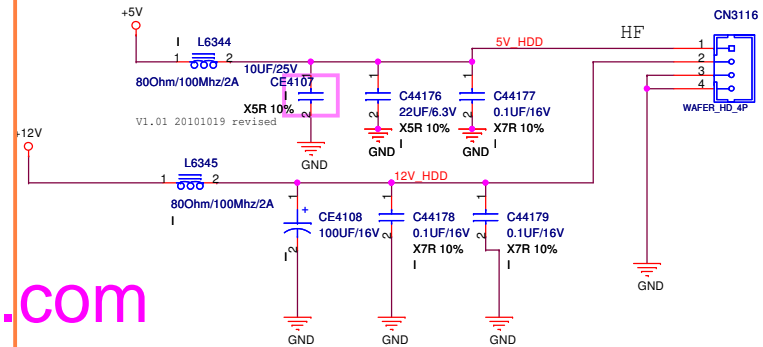
1.01 20101019 revised



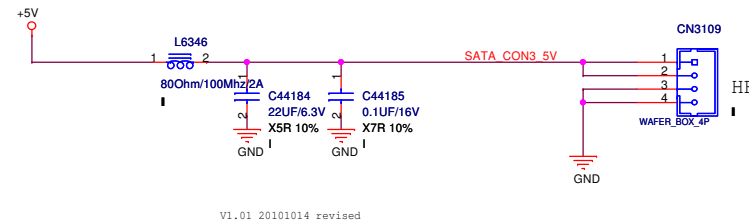
SATA CONTROLLER #2
(SLAVE)

COLOR = WHITE

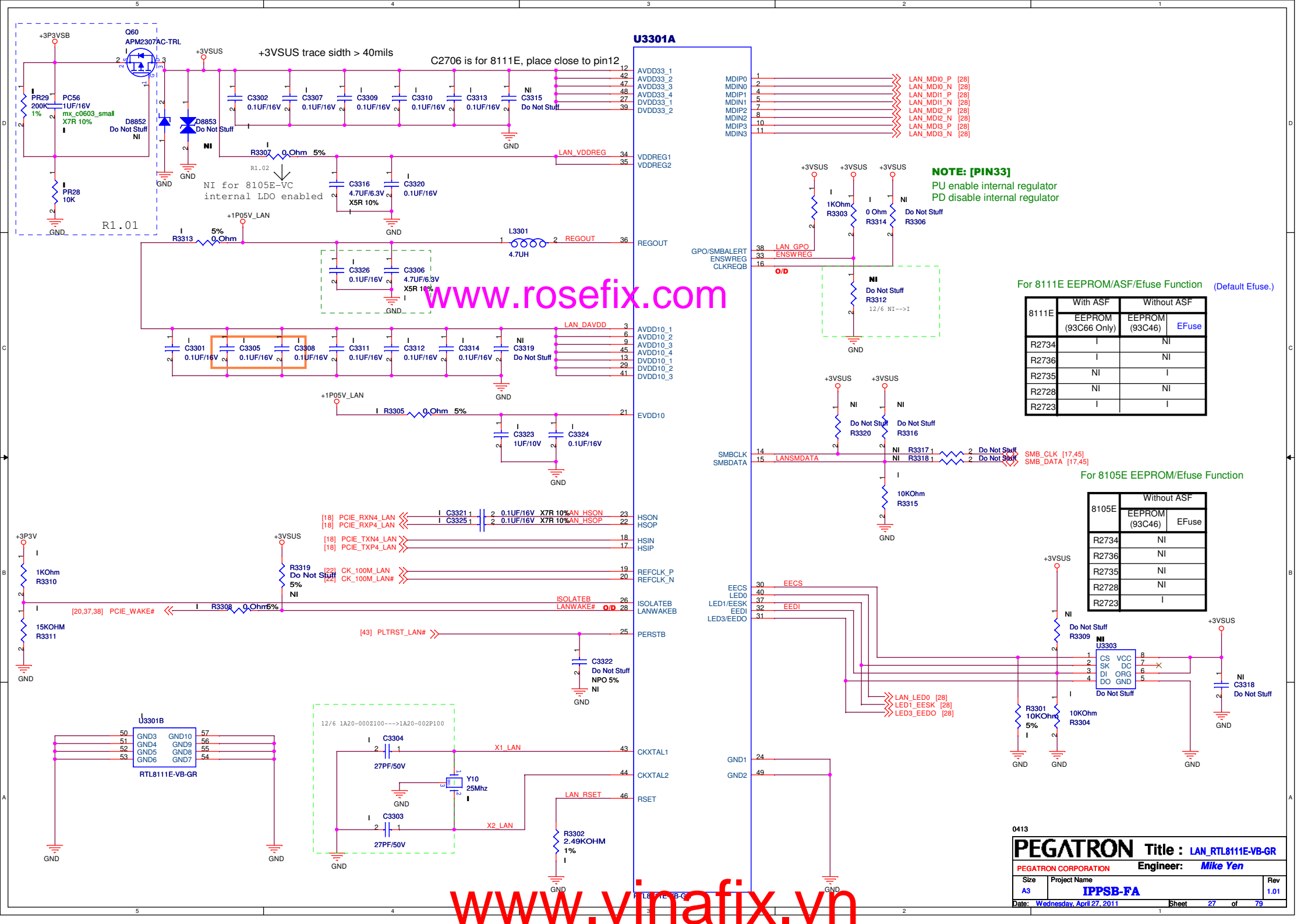
SATA POWER CONN.



ODD POWER CONN.



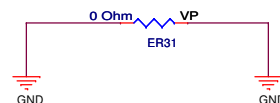
www.vinafix.vn



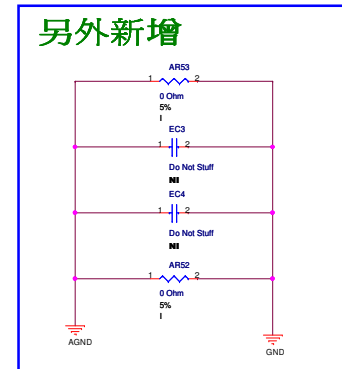
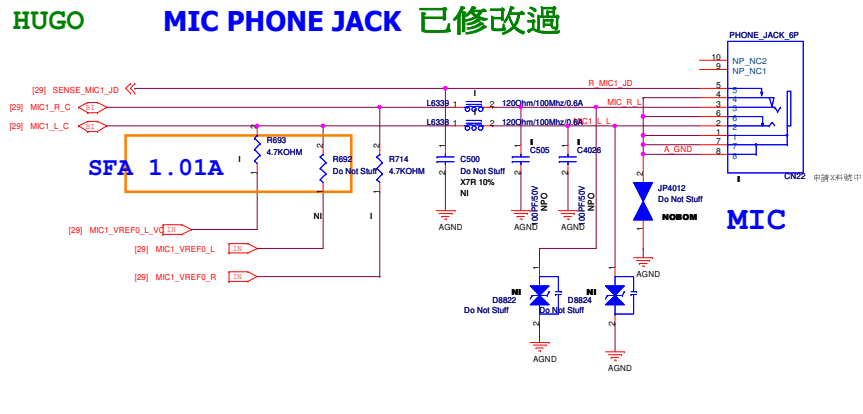
www.rosefix.com

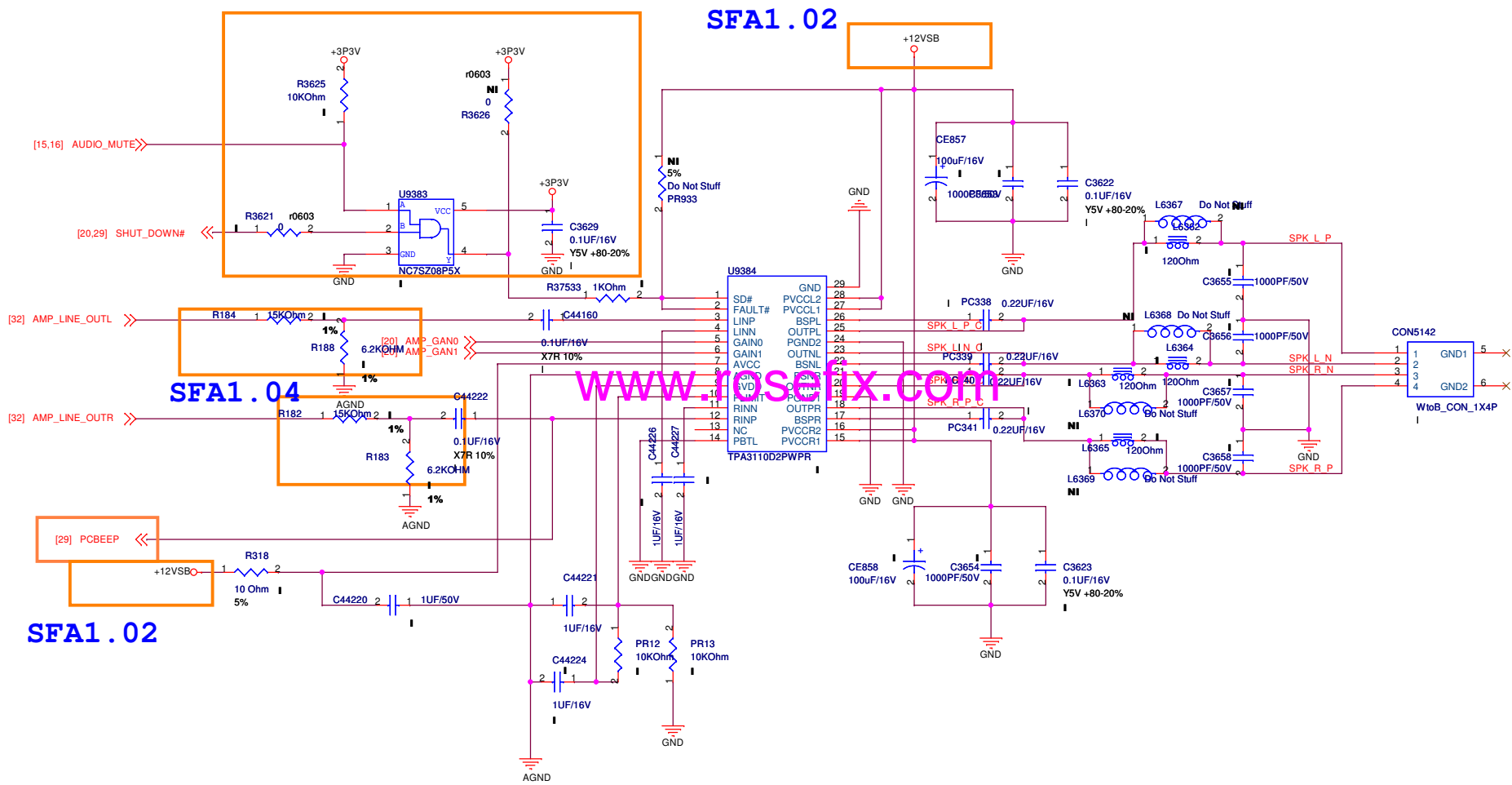


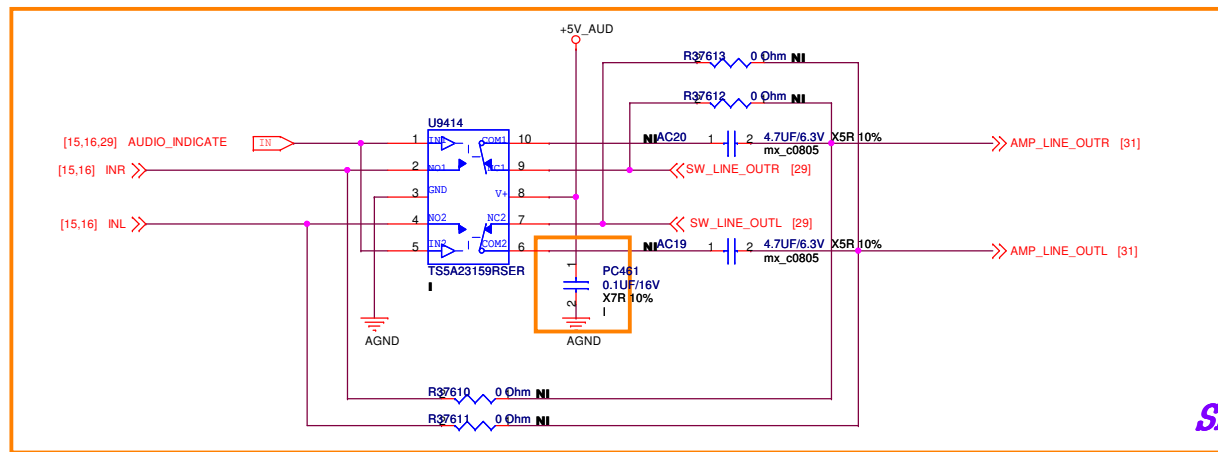
State	LINK Green LED	Yellow LED ACTIVE
S0	ON	OFF or blinking
S1,S3,S4	OFF	OFF



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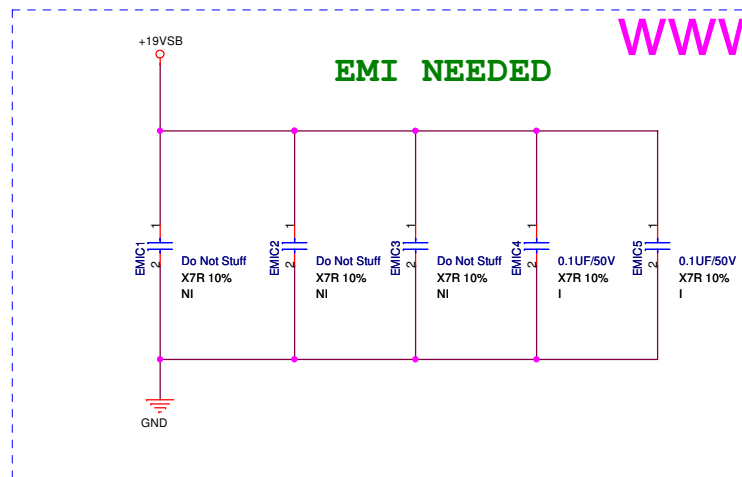




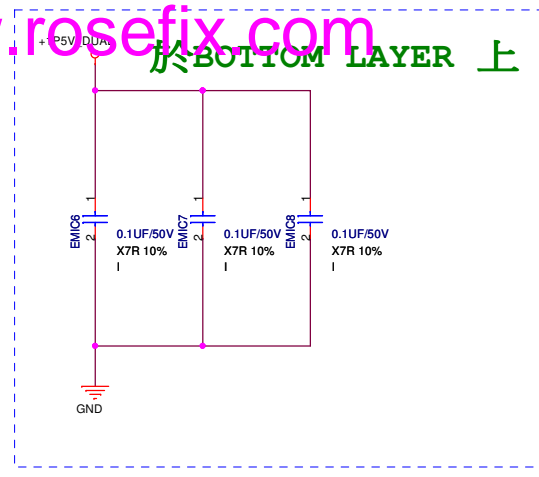


SFA1.04

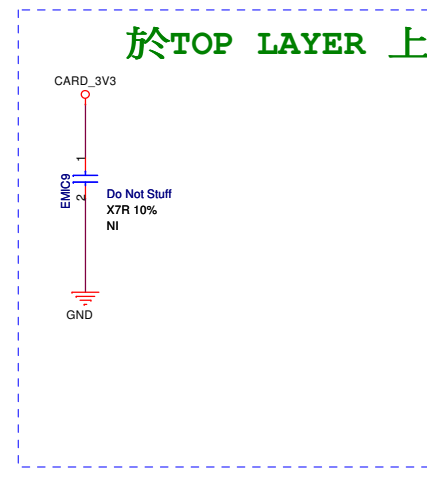
www.rosefix.com



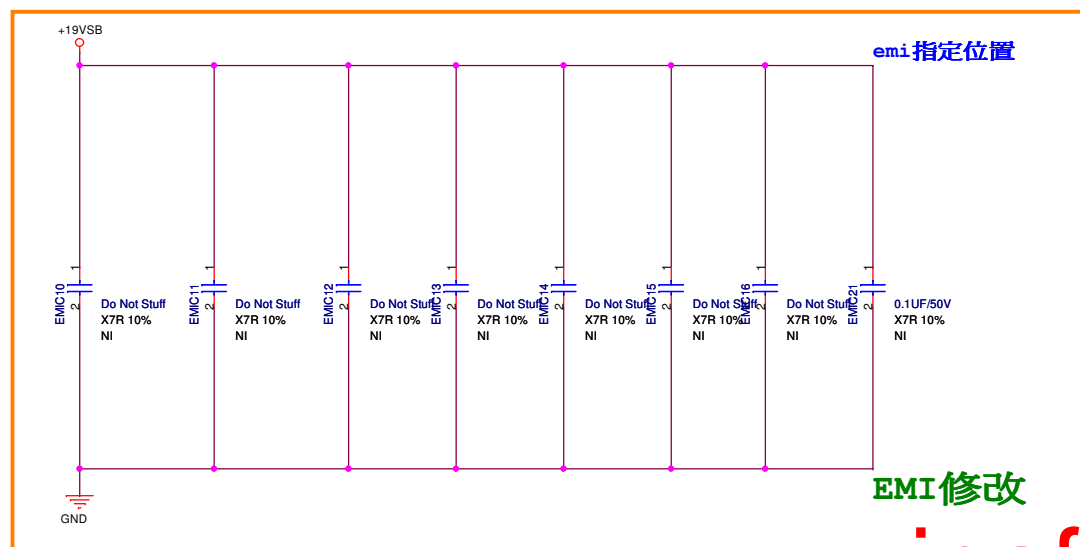
EMI NEEDED



於BOTTOM LAYER 上

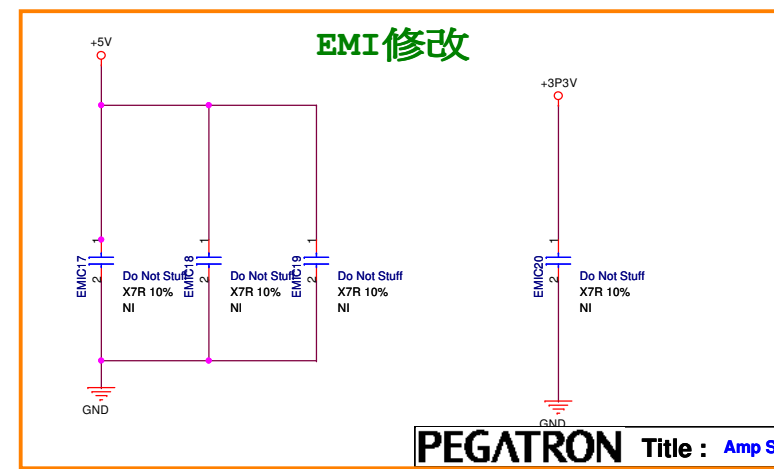


於TOP LAYER 上



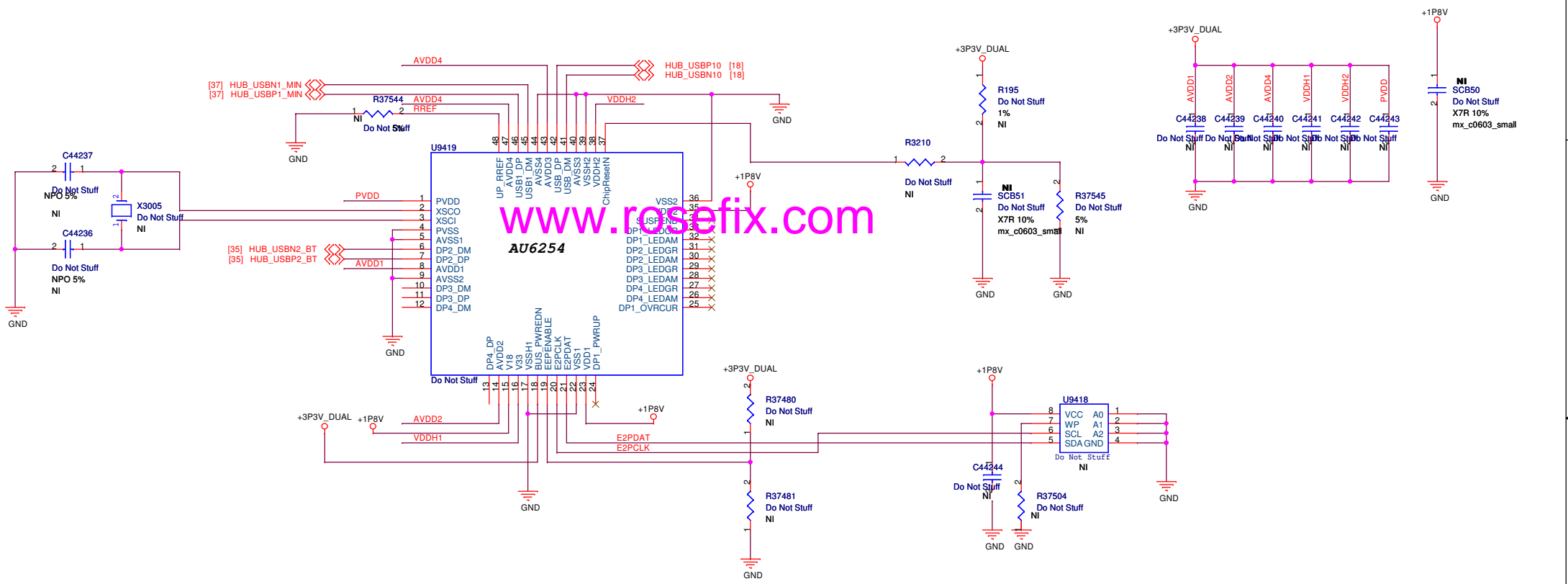
emi指定位置

EMI修改



EMI修改

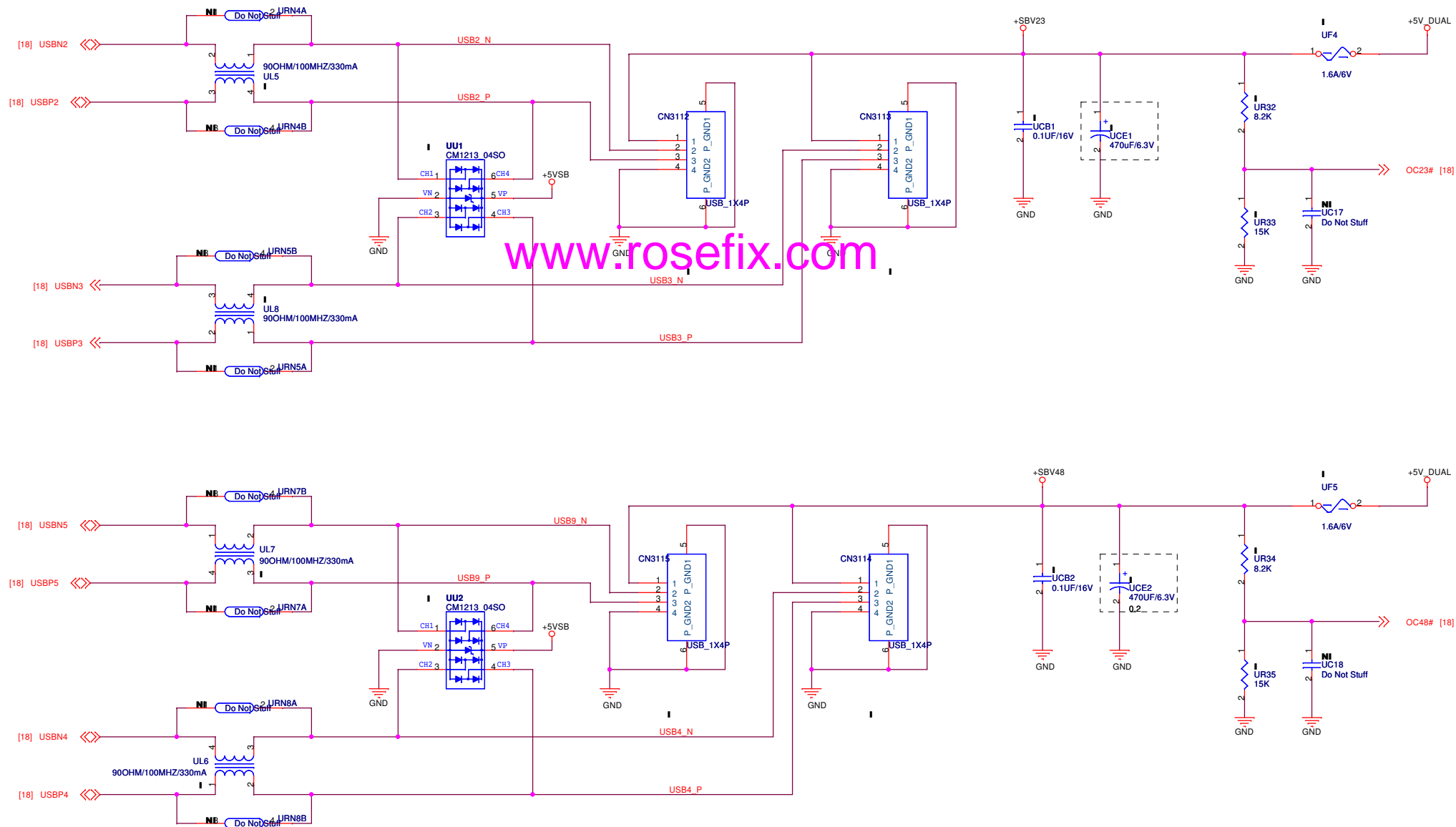
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整頁修改過

Rear USB2.0 *4

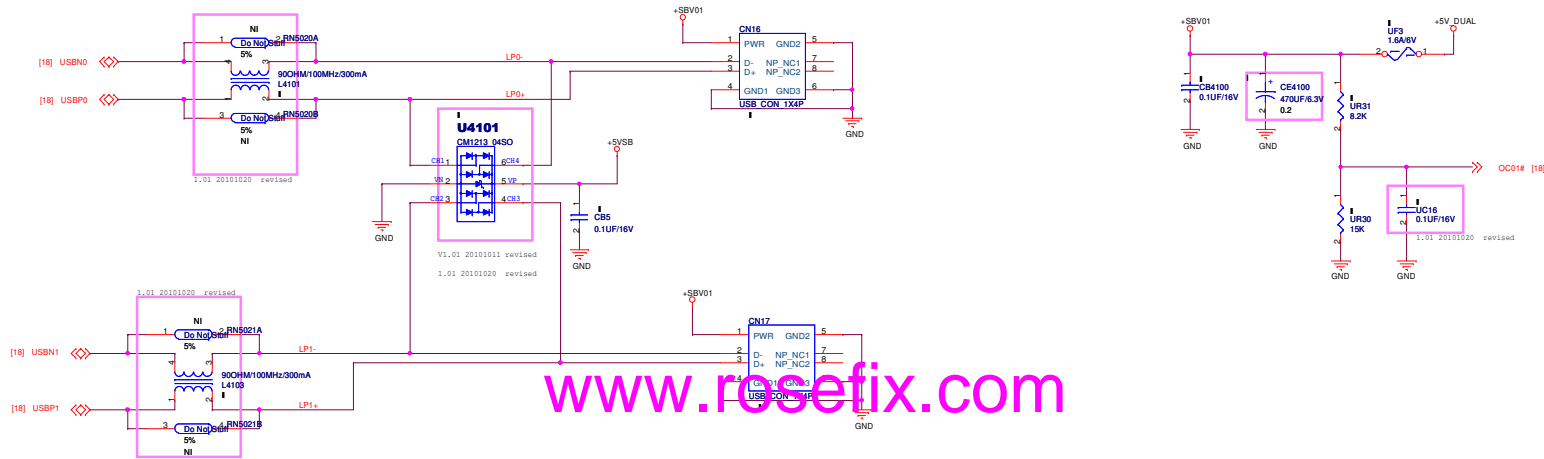


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PEGATRON		Title : Rear USB	
PEGATRON CORPORATION		Engineer: Mike Yen	
Size A3	Project Name IPPSB-FA	Rev 1.01	
Date: Wednesday, April 27, 2011		Sheet 34	of 79

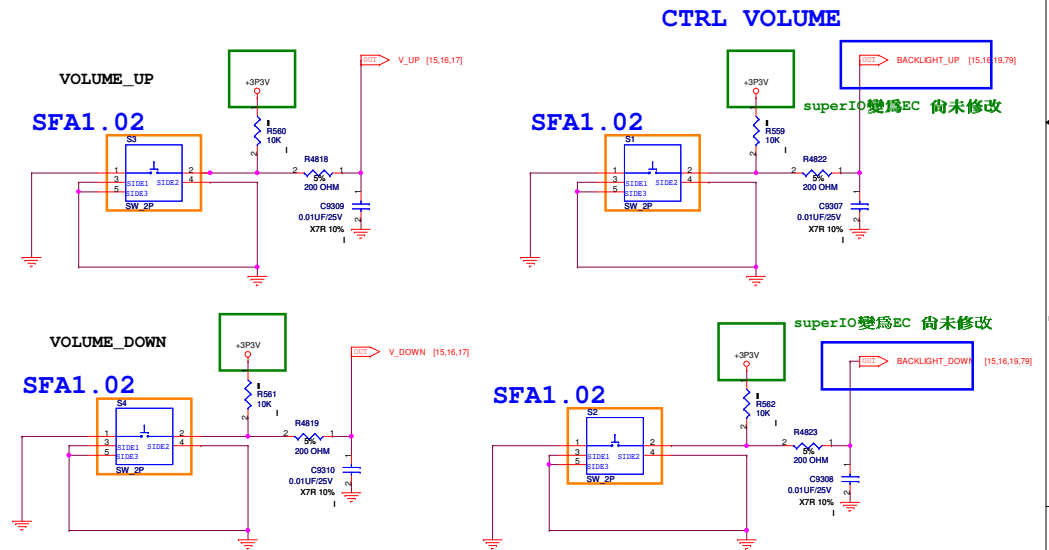
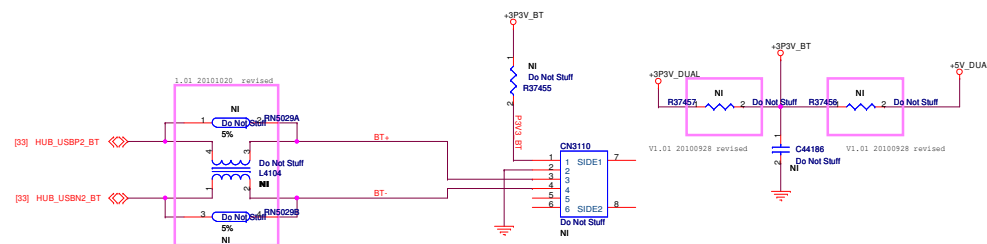
Side USB

已修改過



另外增加
Internal I/O
BLUE TOOTH

the DMC device connected BT symbols is needed

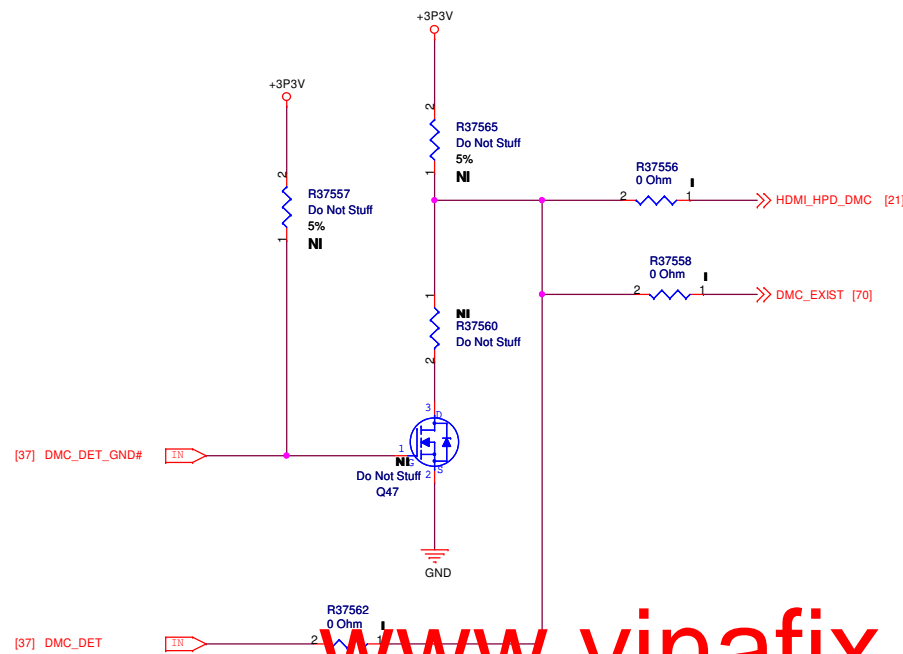
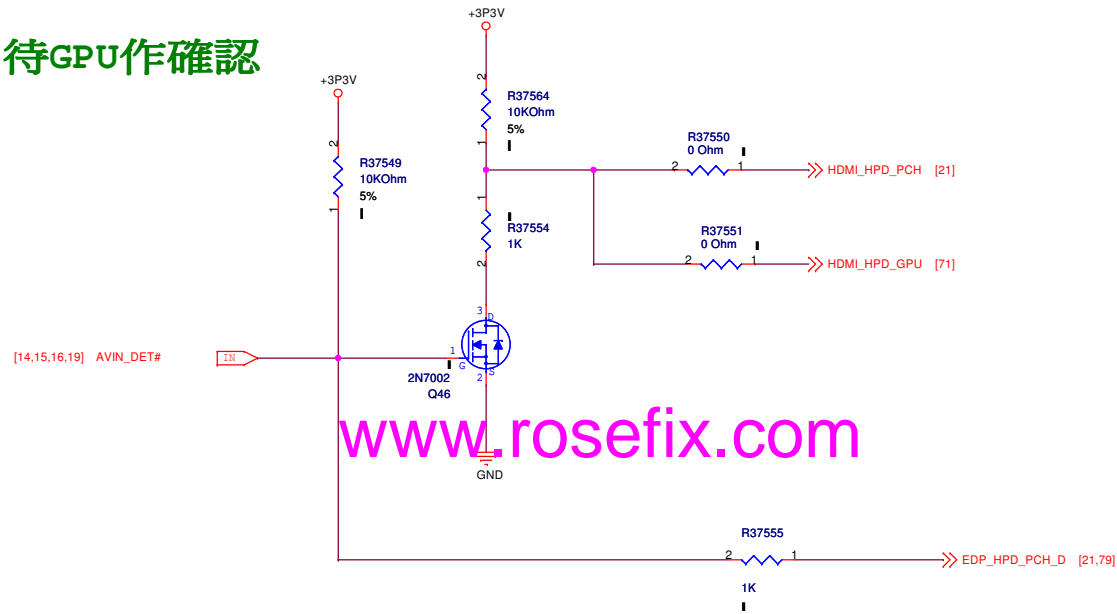


0413

PEGATRON		Title : Side USB&BT	
PEGATRON CORPORATION		Engineer: Mike Yen	
Size	Project Name		Rev
A2	IPPSB-FA		1.01
Date: Wednesday, April 27, 2011		Sheet 35 of 79	

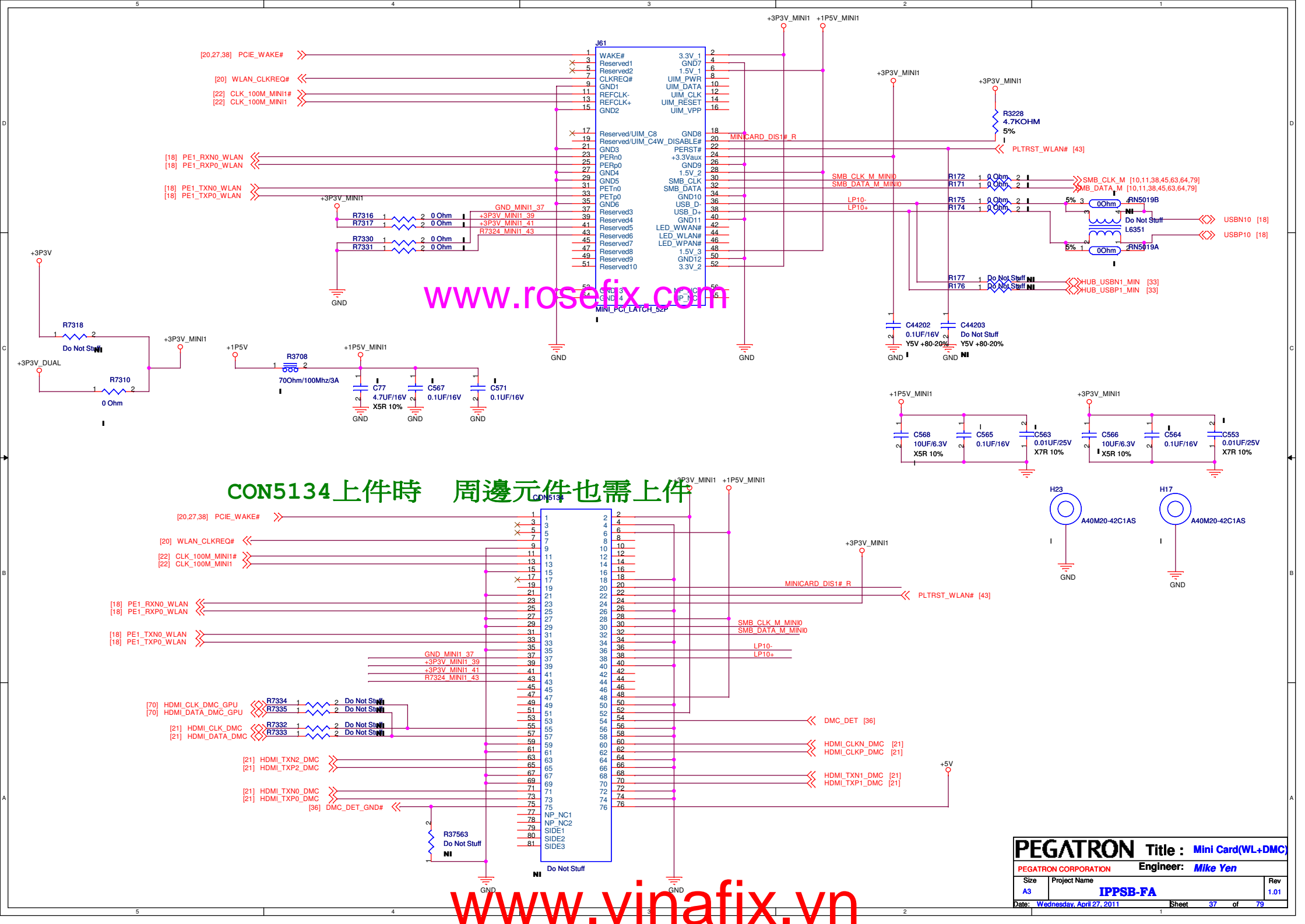
www.vinafix.vn

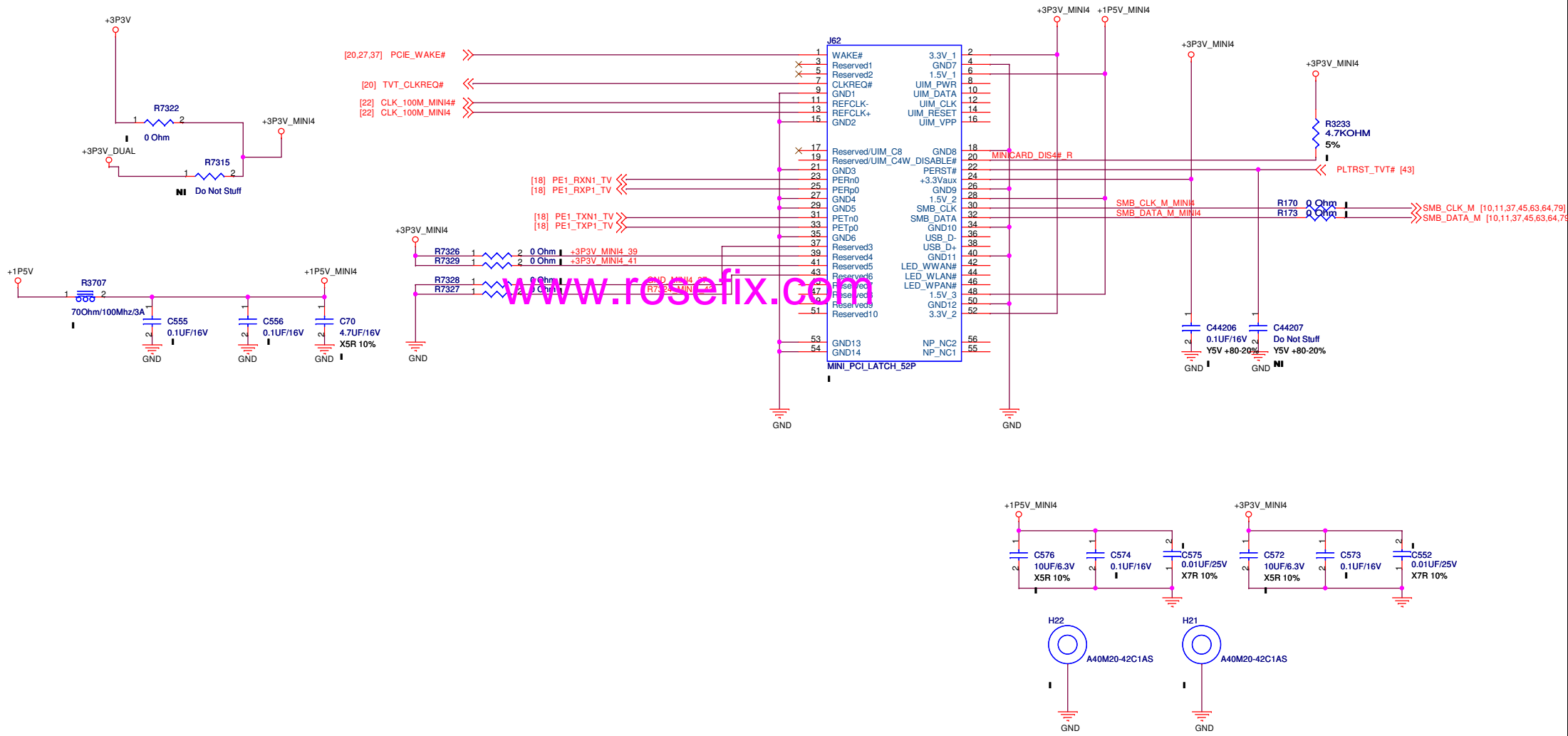
待GPU作確認



0413

PEGATRON		Title : HPD DET	
R&D 2		Engineer: Jerry, Hsuan	
Size	Project Name	Rev	
A3	IPPSB-FA	1.01	
Date: Wednesday, April 27, 2011		Sheet	36 of 79

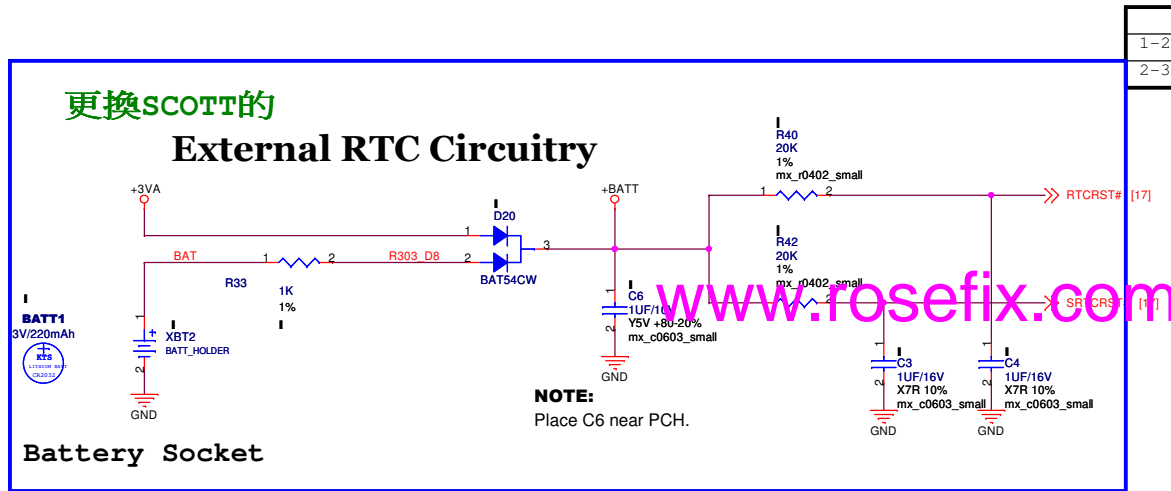




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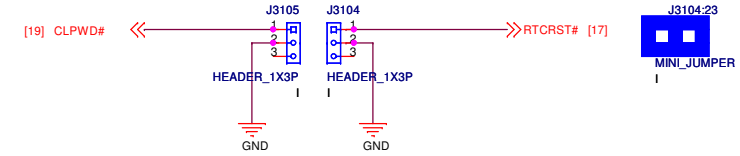
CLR CMOS CIRCUIT

CLR PASSWORD CIRCUIT



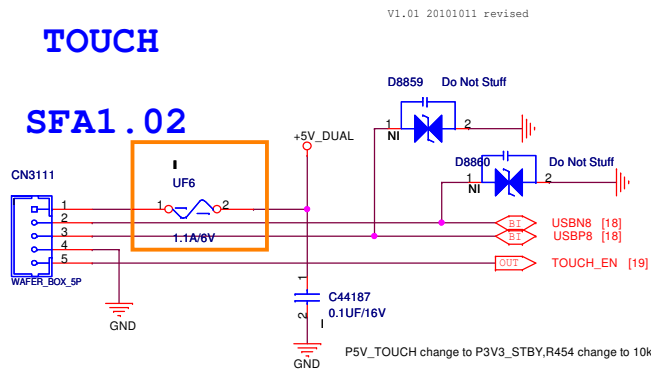
	PASSWORD
1-2	CLEAR
2-3	Default

	CMOS RTC
1-2	CLEAR
2-3	Default



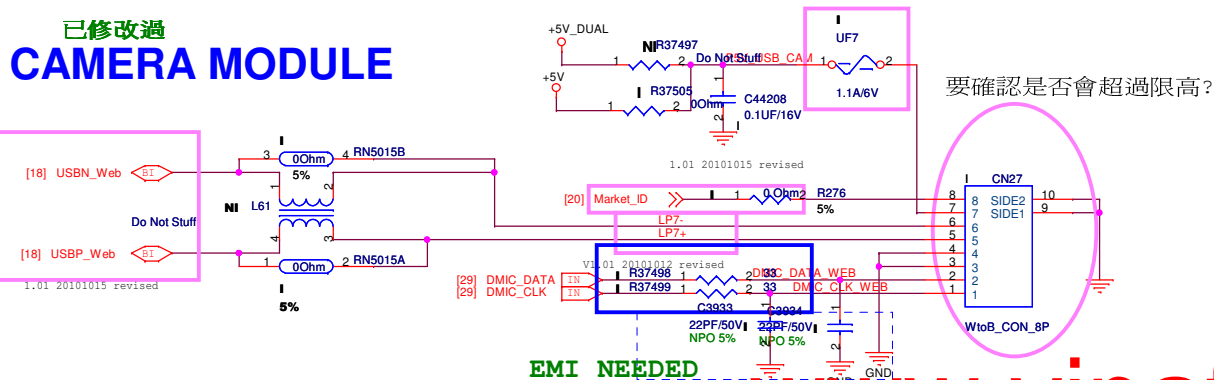
TOUCH

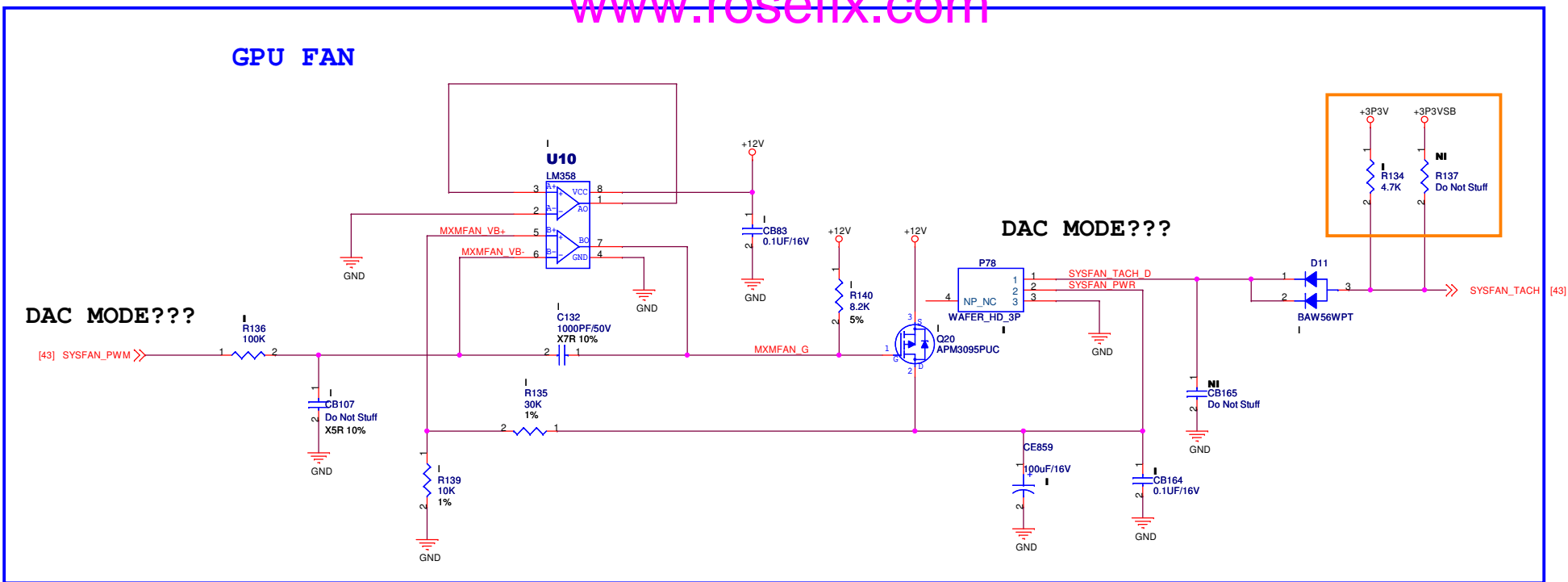
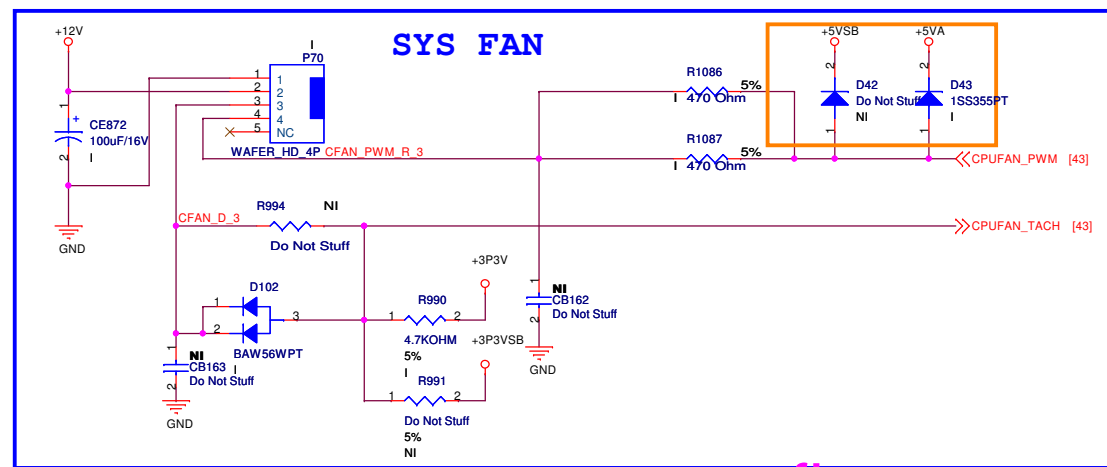
SFA1.02



SFA1.03

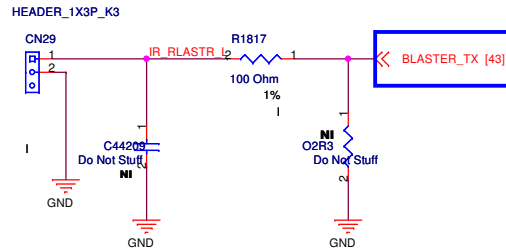
已修改過
CAMERA MODULE





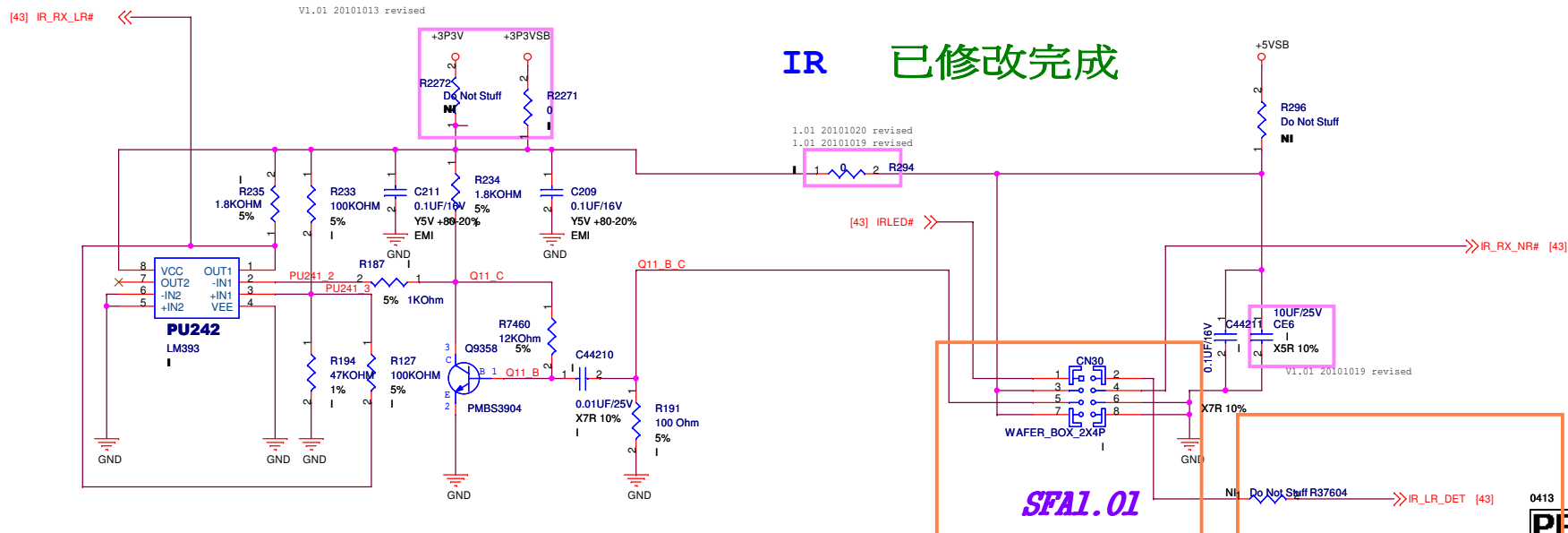
線條未改

IR Blaster



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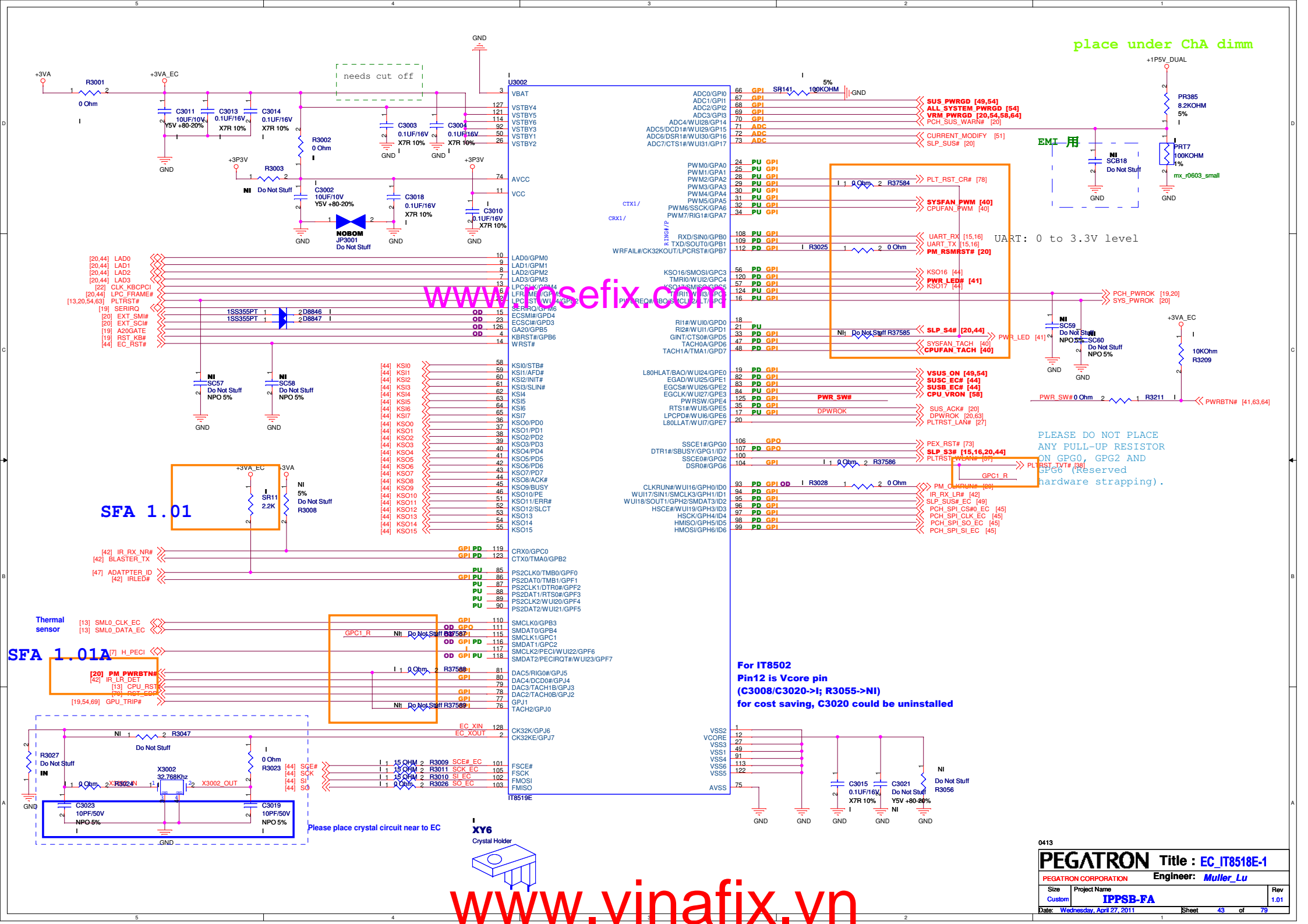
IR 已修改完成



SFA1.01

SFA1.01A

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place under ChA dimm

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PLEASE DO NOT PLACE ANY PULL-UP RESISTOR ON GPG0, GPG2 AND GPG6 (Reserved hardware strapping).

For IT85102
Pin12 is Vcore pin
(C3008/C3020->I; R3055->NI)
for cost saving, C3020 could be uninstalled

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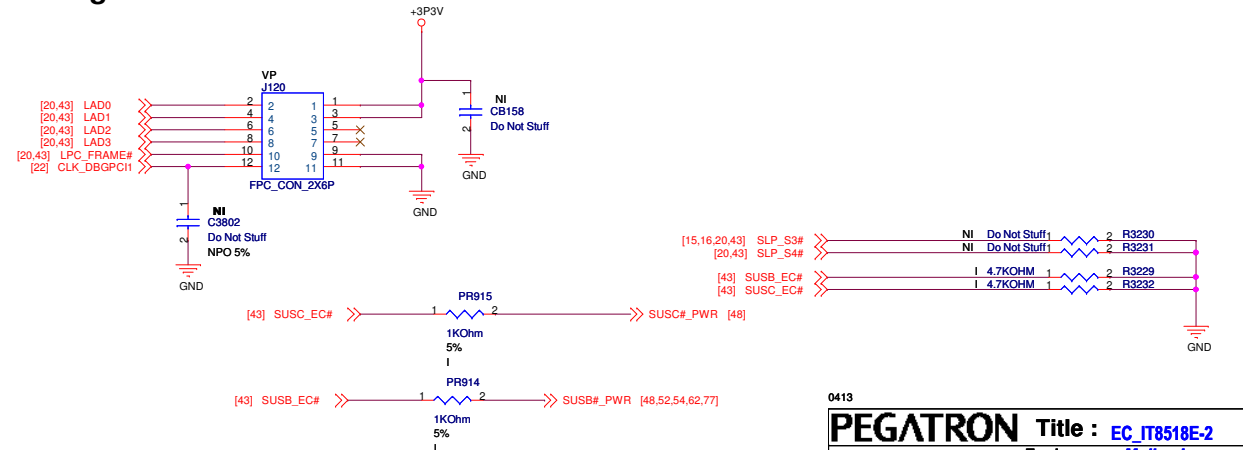
[illegible]

For Instant Key & Switch

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[illegible]

The diagram shows the electrical path for the FORCE_OFF# signal. It starts with a red input signal, passes through a pull-up resistor to +3VA, then through a diode (D3108) to a purple signal line. This line has another pull-up resistor to +3VA_EC, followed by another diode (D3107) and a decoupling capacitor (C3103) to ground. The final output is the EC_RST# signal, which is blue and labeled 'To EC RESET'.



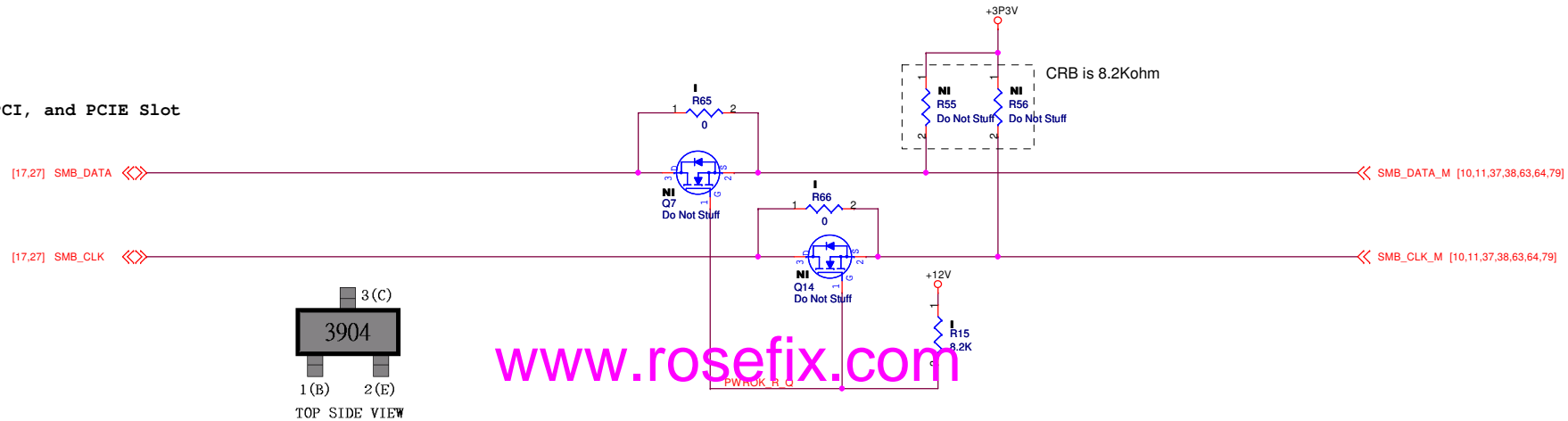
PEGATRON Title : **EC_IT8518E-2**

Size	Project Name	Re
Custom	IPPSB-FA	1.0

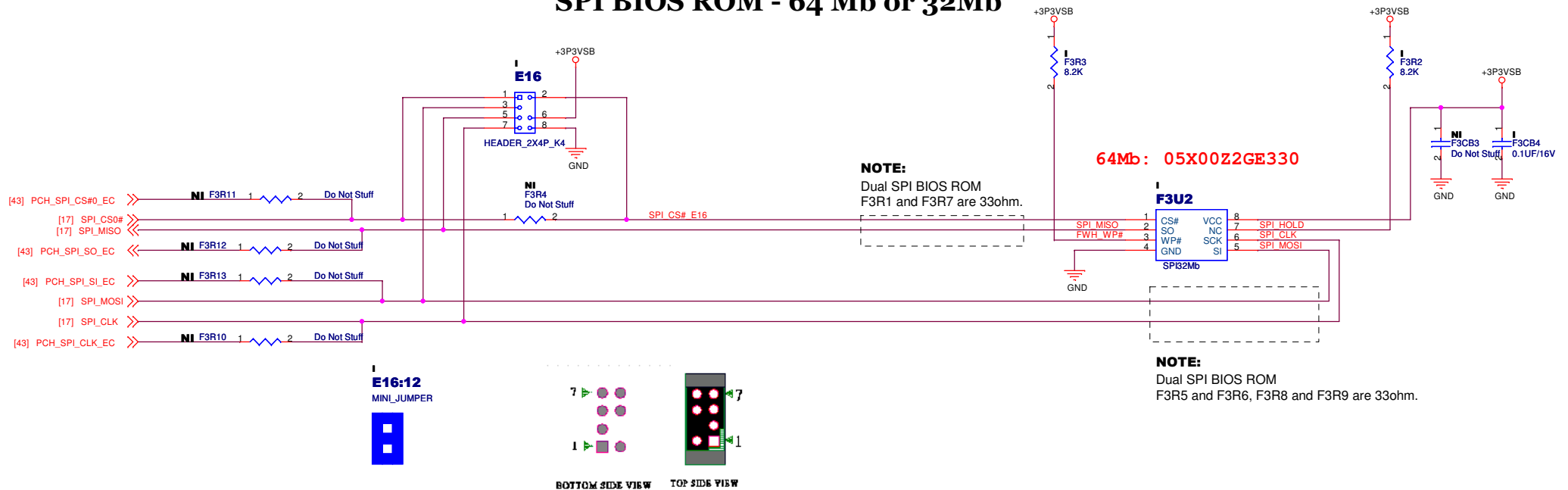
Date: Wednesday, April 27, 2011 Sheet 44 of 79

SM BUS Control

To PCH, PCI, and PCIE Slot



SPI BIOS ROM - 64 Mb or 32Mb



PEGATRON DT-MB RESTRICTED SECRET

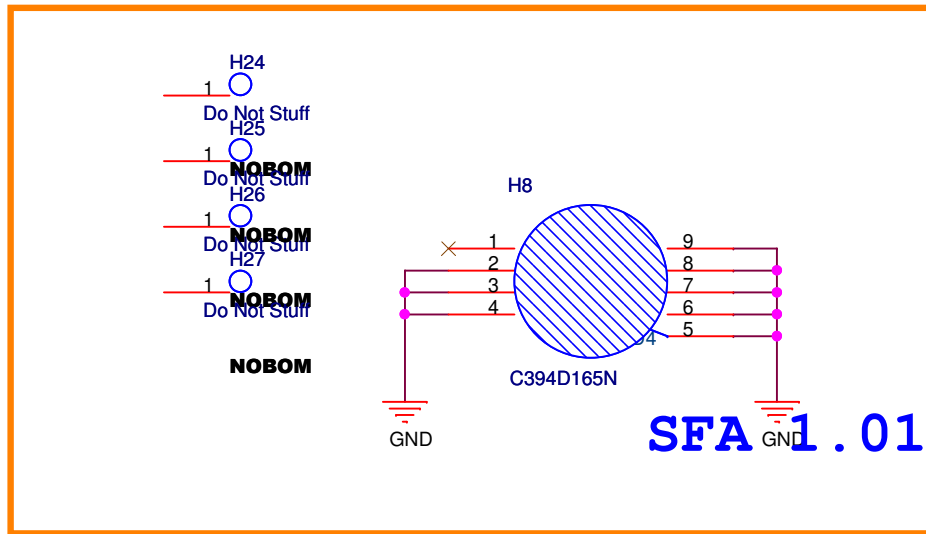
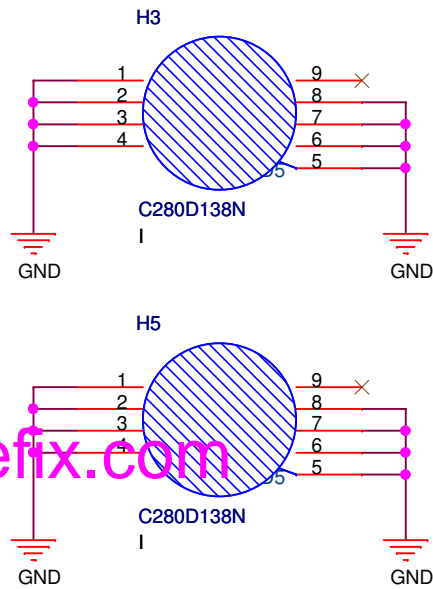
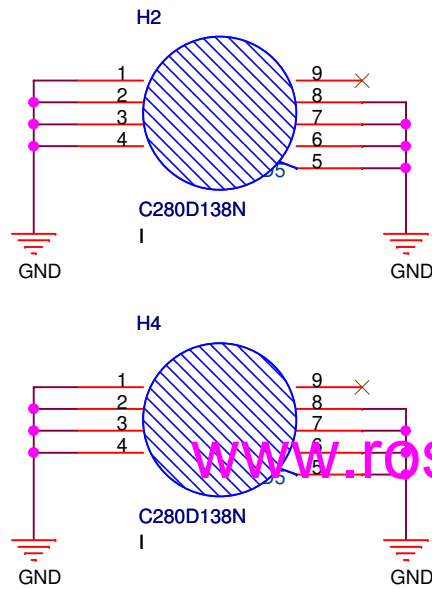
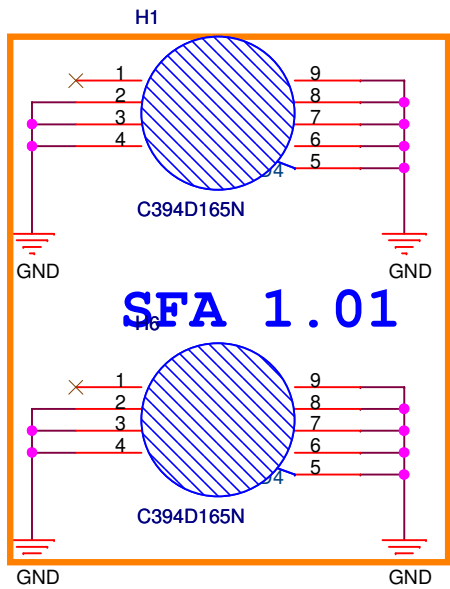
PEGATRON Title : **SM BUS & SPI ROM**

PEGATRON CORPORATION Engineer: XXXX-XX

Size	Project Name	Rev
------	--------------	-----

A3	IPPSB-FA	1.01
Date: Wednesday, April 27, 2011		
Sheet 45 of 70		

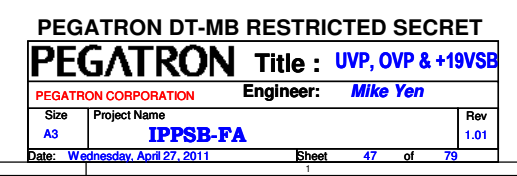
Date: Wednesday, April 27, 2011	Street: 45	Or: 79
1		



0413

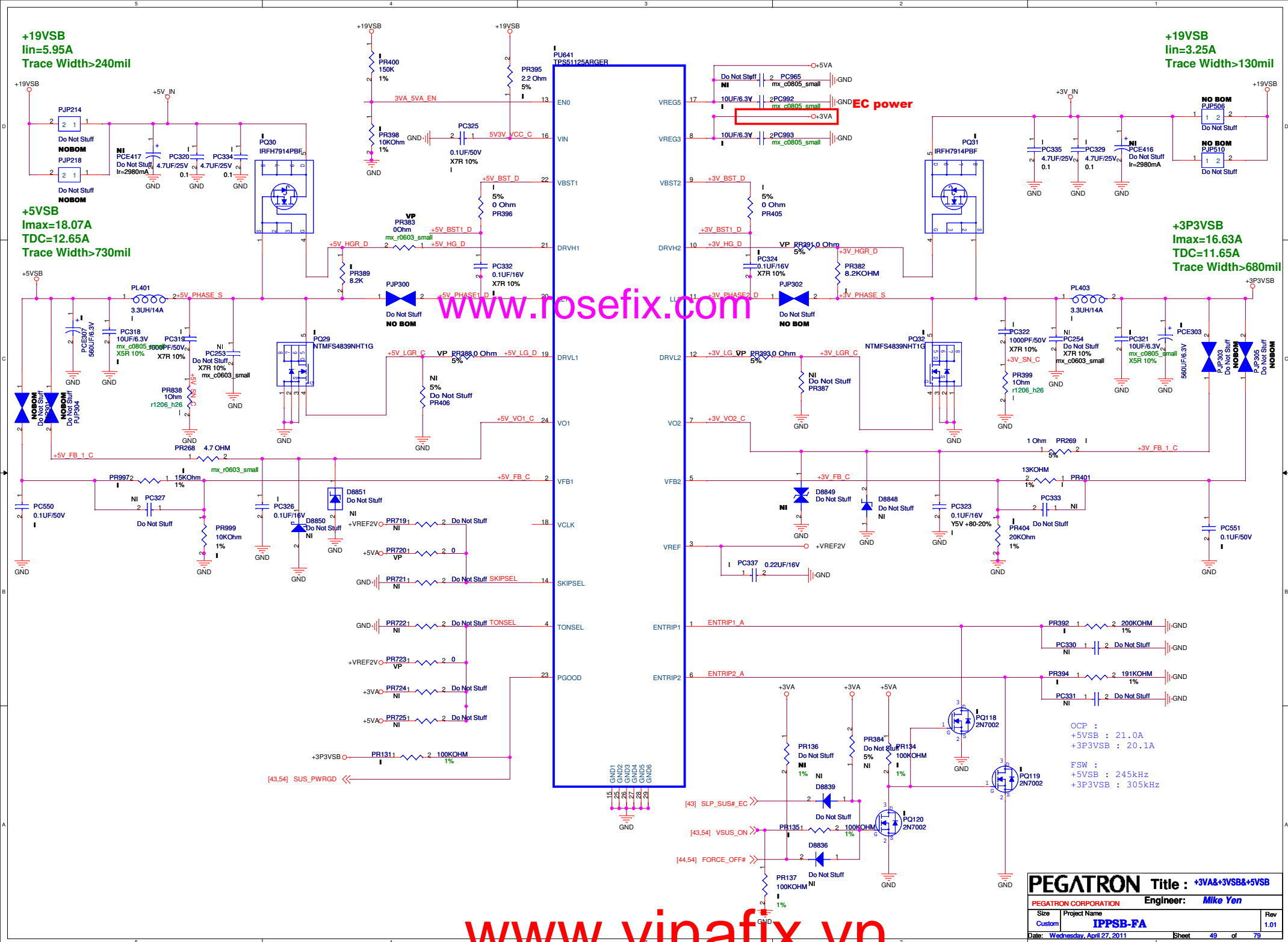
PEGATRON		Title : SCREW HOLE	
PEGATRON CORPORATION		Engineer: Mike Yen	
Size A	Project Name IPPSB-FA		Rev 1.01
Date: Wednesday, April 27, 2011		Sheet 46	of 79

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+19VSB
lin=5.95A
Trace Width>240mil

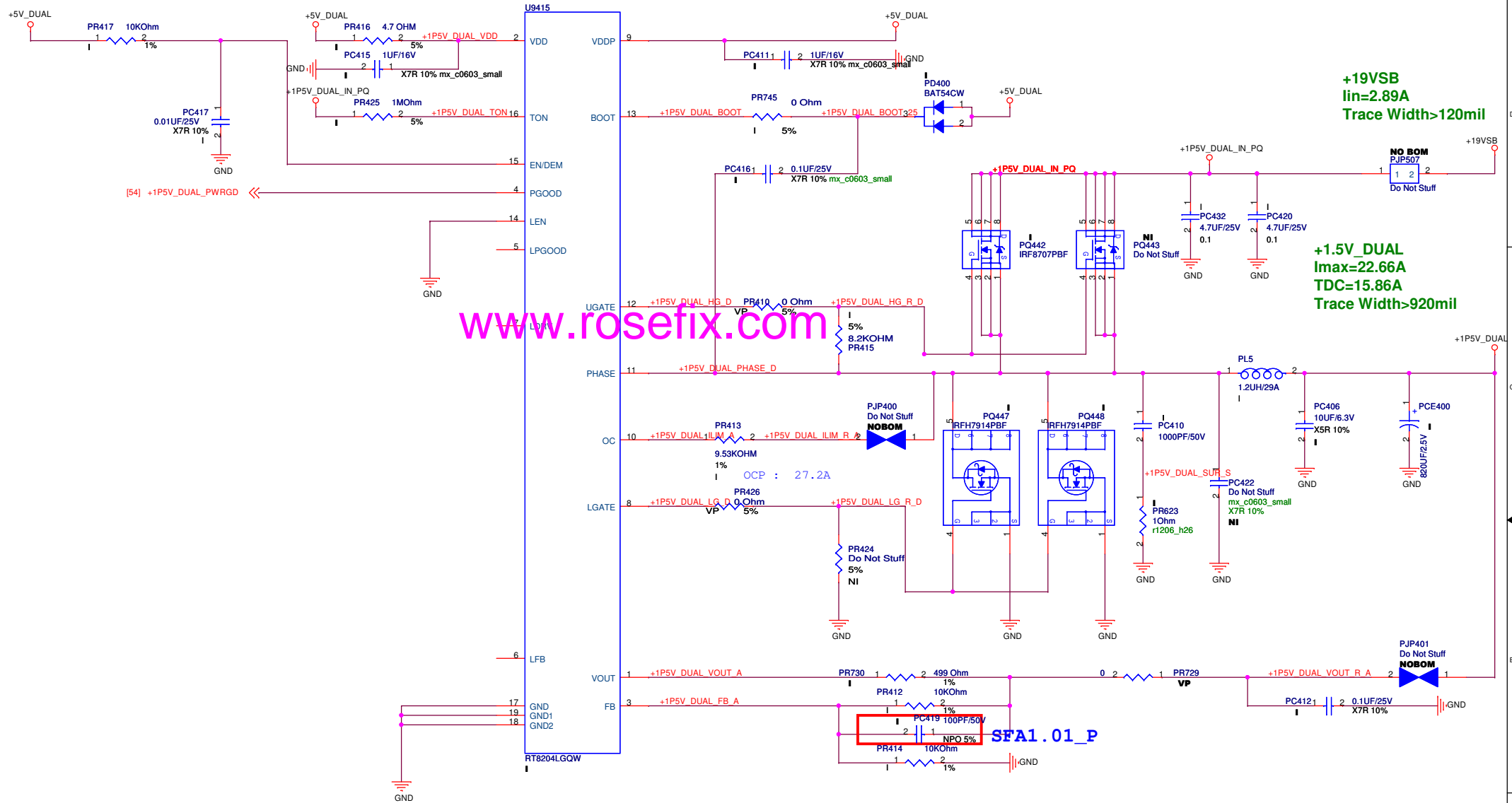
+19VSB
lin=3.25A
Trace Width>130mil



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www.vinafix.vn

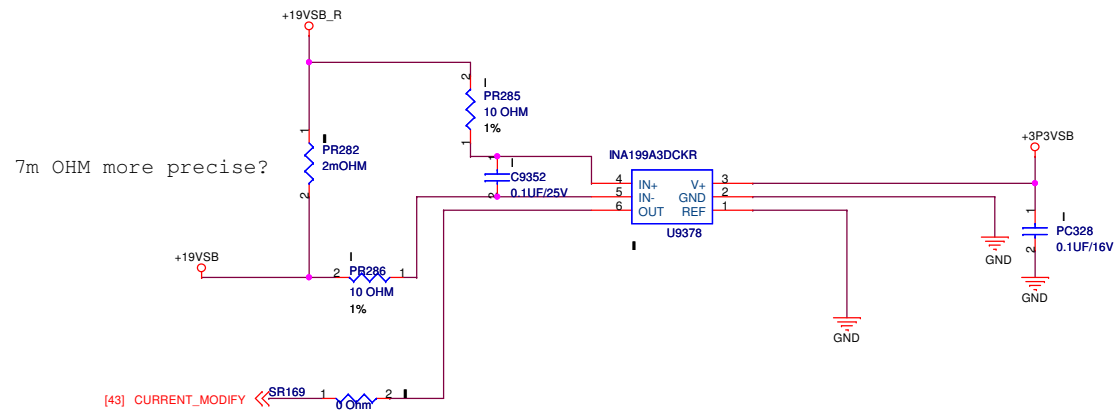


+19VSB
Iin=2.89A
Trace Width>120mil

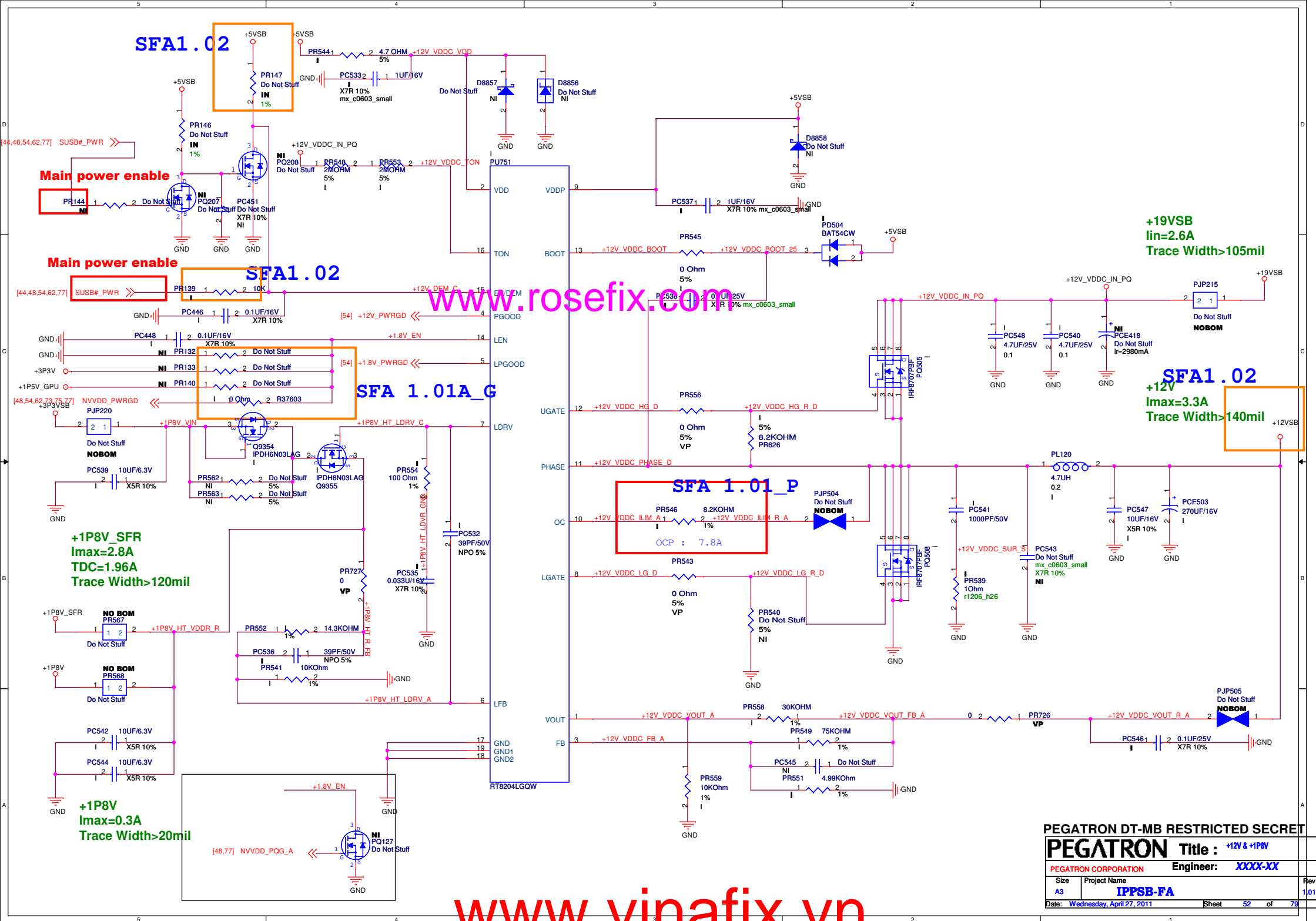
+1.5V_DUAL
I_{max}=22.66A
TDC=15.86A
Trace Width>920mil

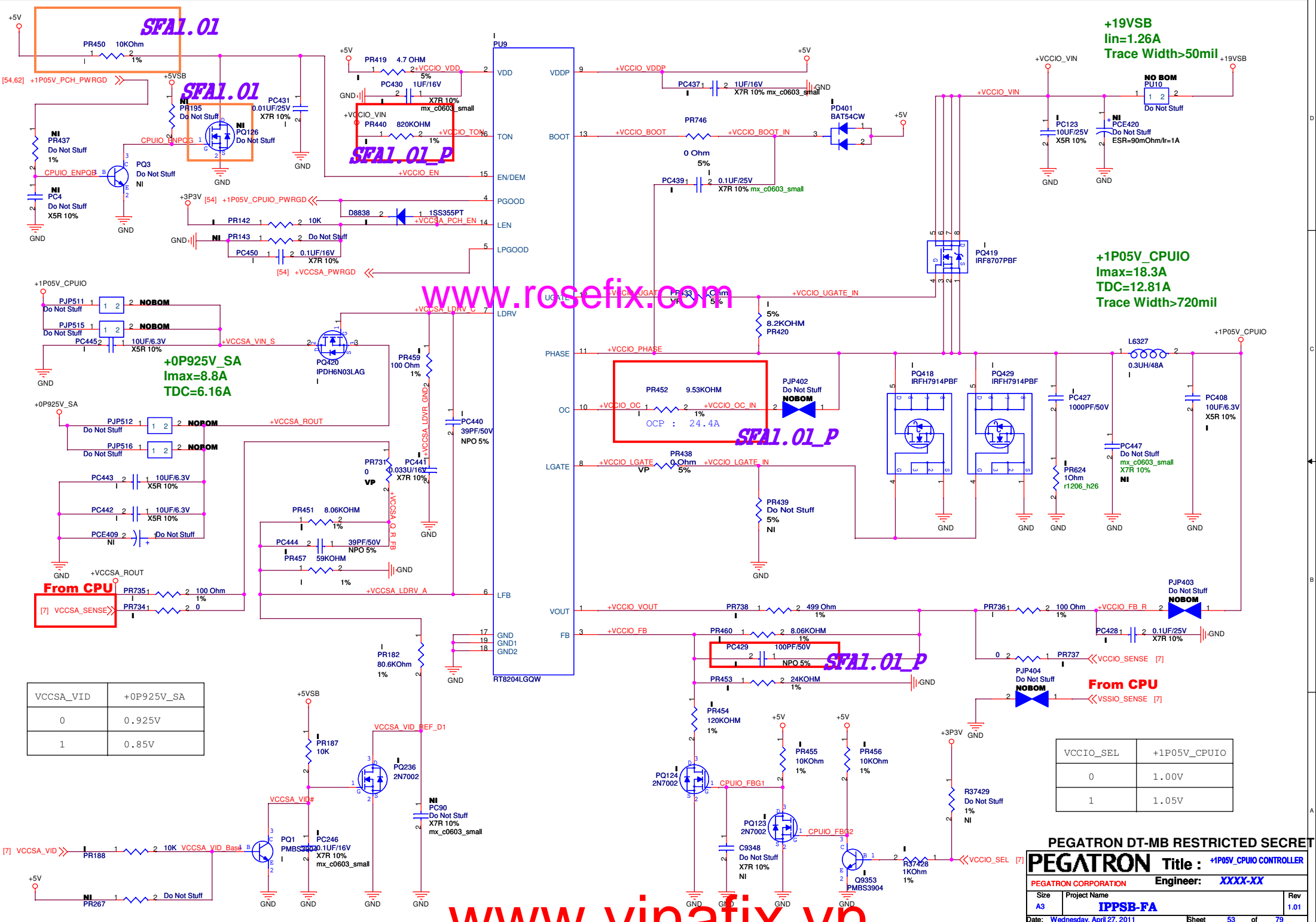
SFA1.01_P

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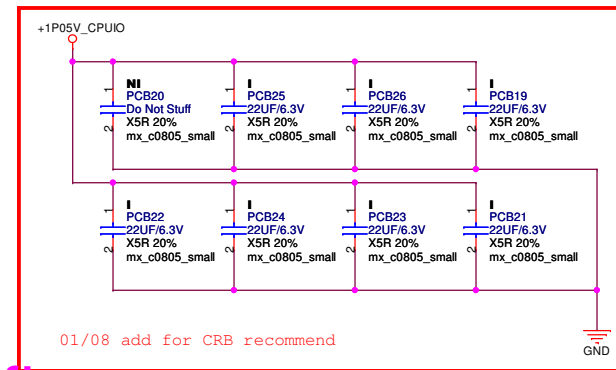
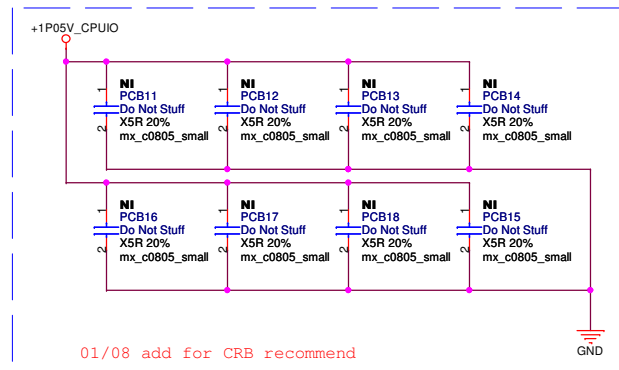
www.vinafix.vn



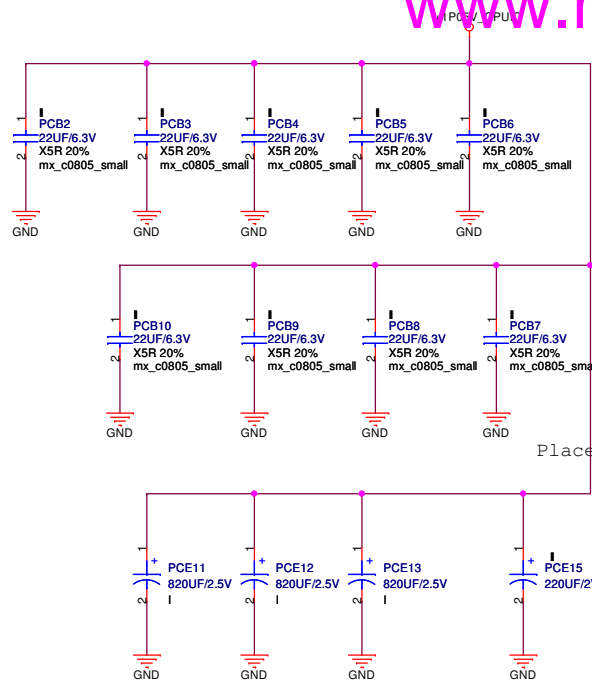


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VCCIO Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	3	7mΩ	1.4nH	Output	Various. See layout figures	1
22µF 0805 X5R	9	5mΩ	0.55nH	Output	Inside processor socket cavity	1, 2, 3
0805 placeholders	16				Backside	

PEGATRON DT-MB RESTRICTED SECRET

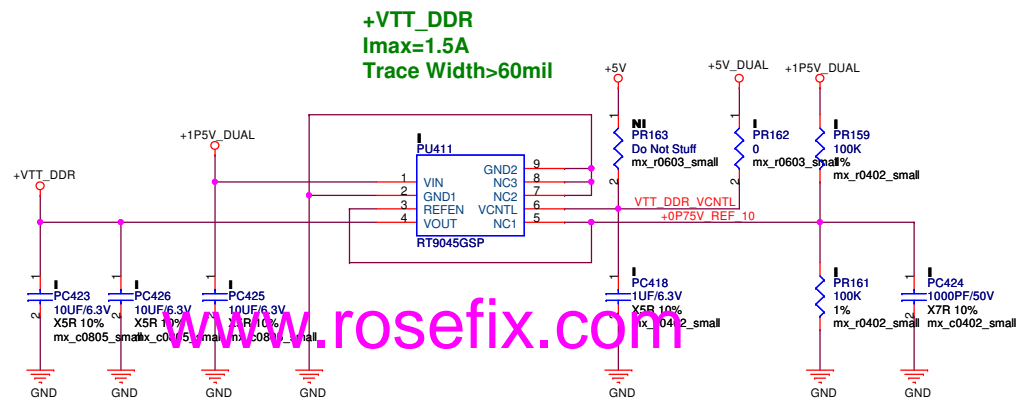
PEGATRON Title : 1P05V_CPUIO CAP

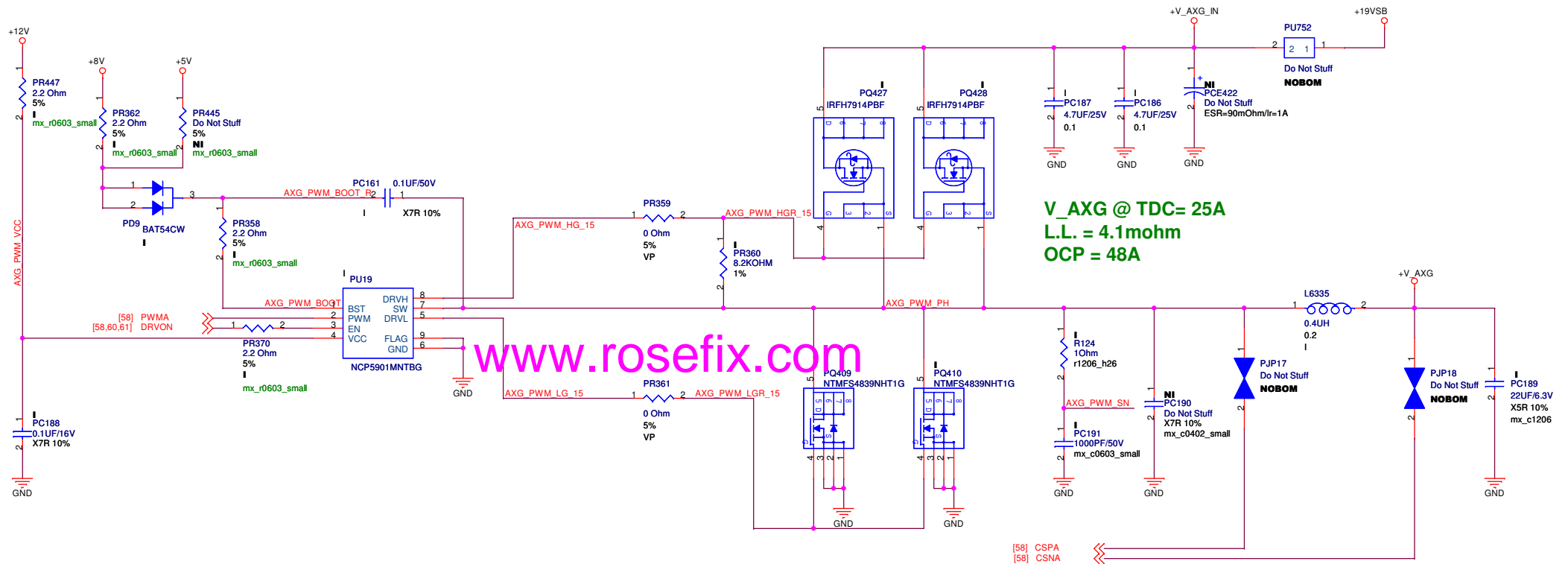
PEGATRON CORPORATION Engineer: XXXX-XX

Size A3 Project Name IPPSB-FA Rev 1.01

Date: Tuesday, April 26, 2011 Sheet 55 of 79

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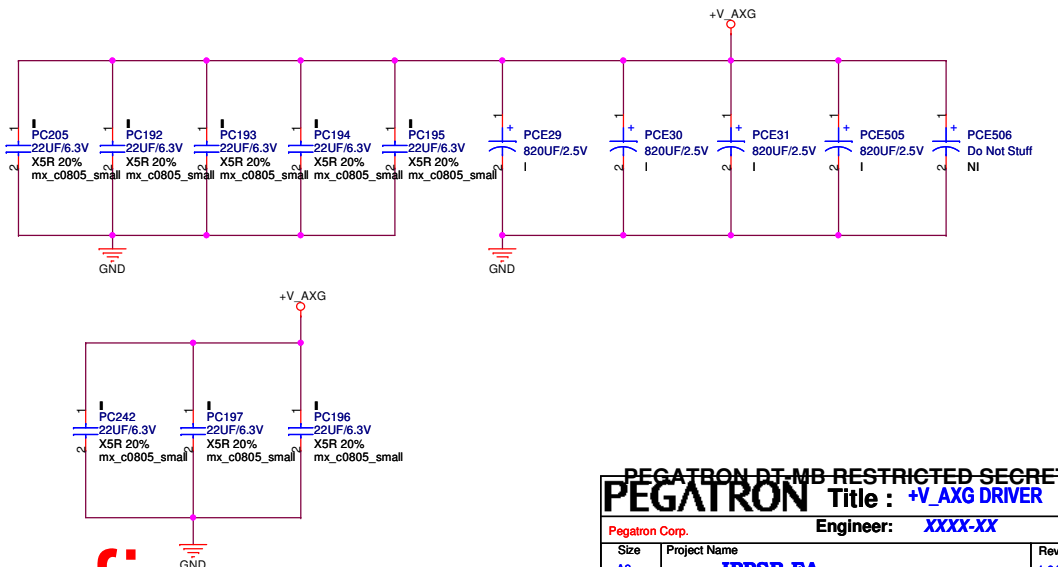


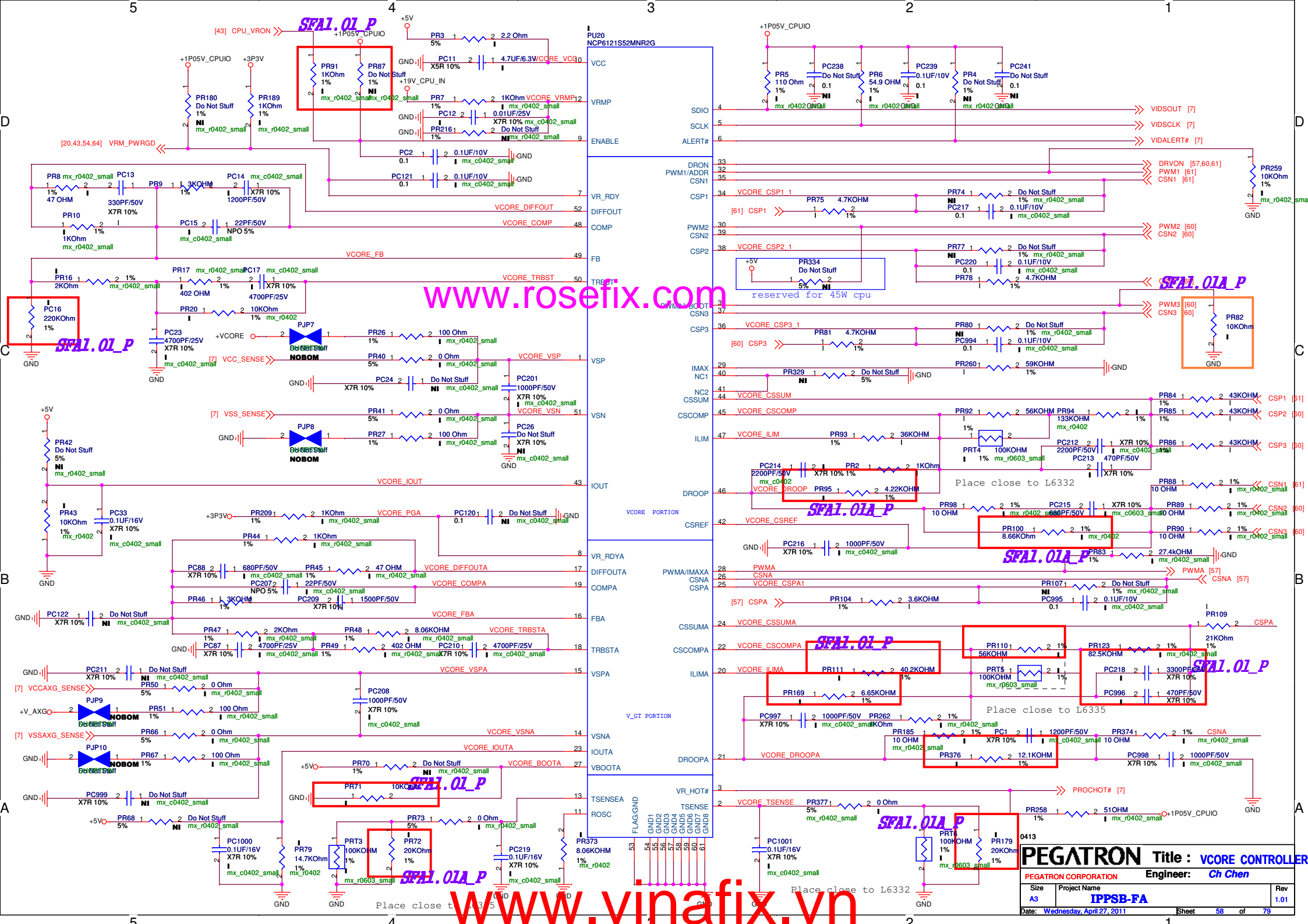
Output CAP

Table 30-4. VCCAXG Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	East of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	6	5mΩ	0.55nH	Output	4 - inside processor socket cavity 2(empty) - Bottom of board, near socket	1, 2, 3
4.7µF X5R	3	7mΩ	0.6nH	Input		1

PL-CAP *4
MLCC *6



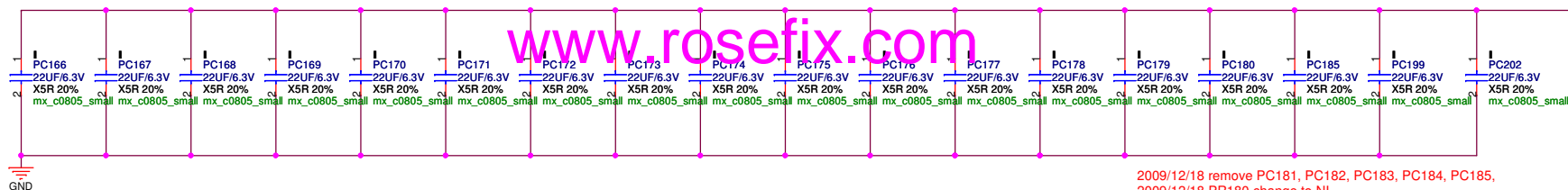
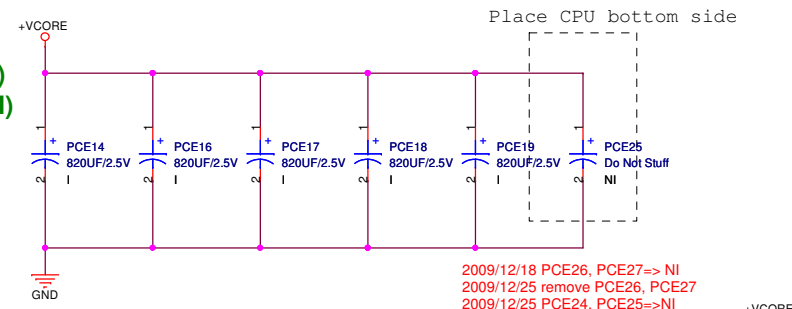


Output CAP

Table 30-2. Decoupling Requirements

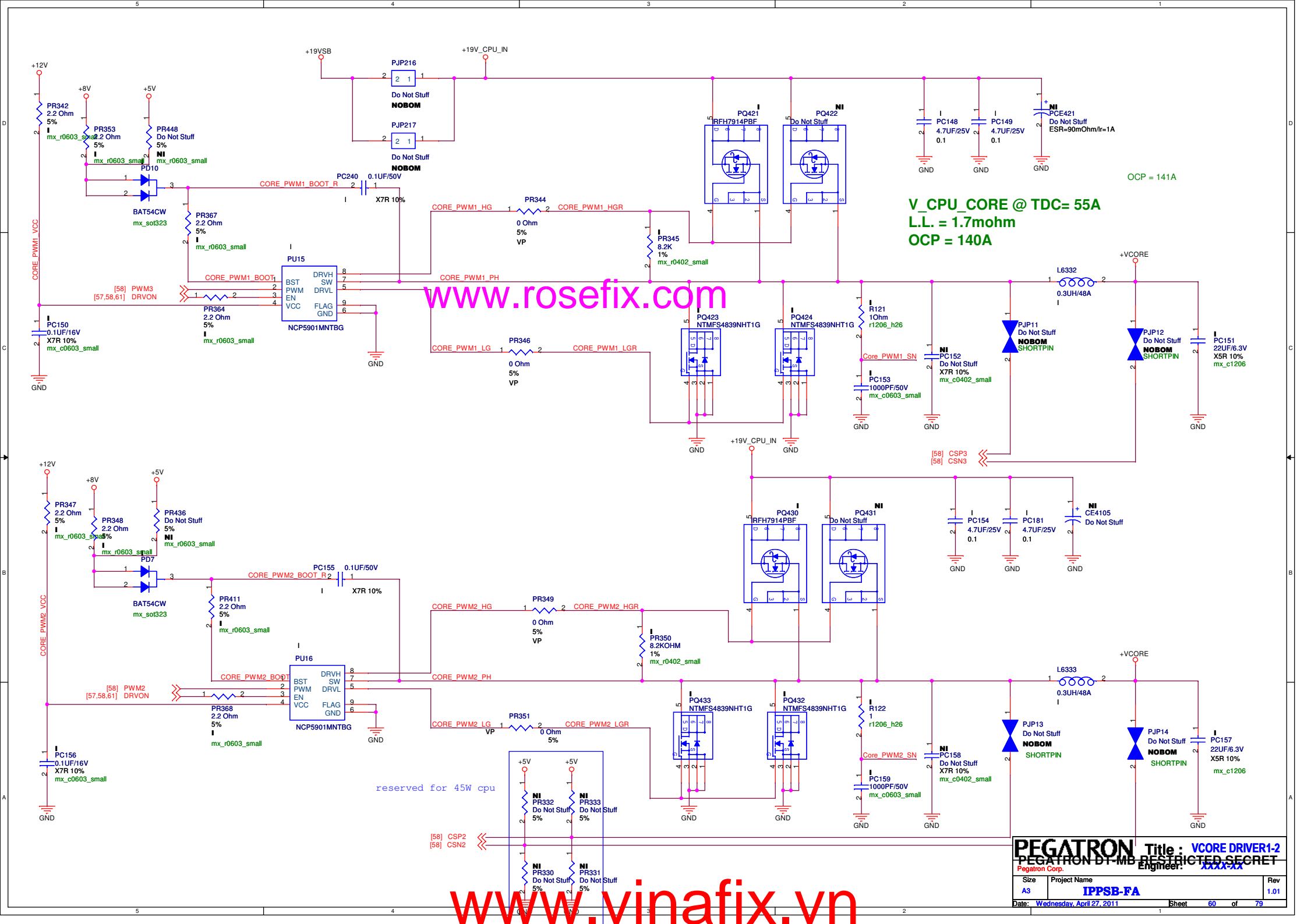
Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	North of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	18	5mΩ	0.55nH	Output	14 - Inside processor socket cavity 4- North of processor - as close to RM keep-out as possible	1, 2 3
Aluminum Electrolytic 390µF	4	51mΩ	6.1nH	Input		1
4.7µF X5R	9	7mΩ	0.6nH	Input		1

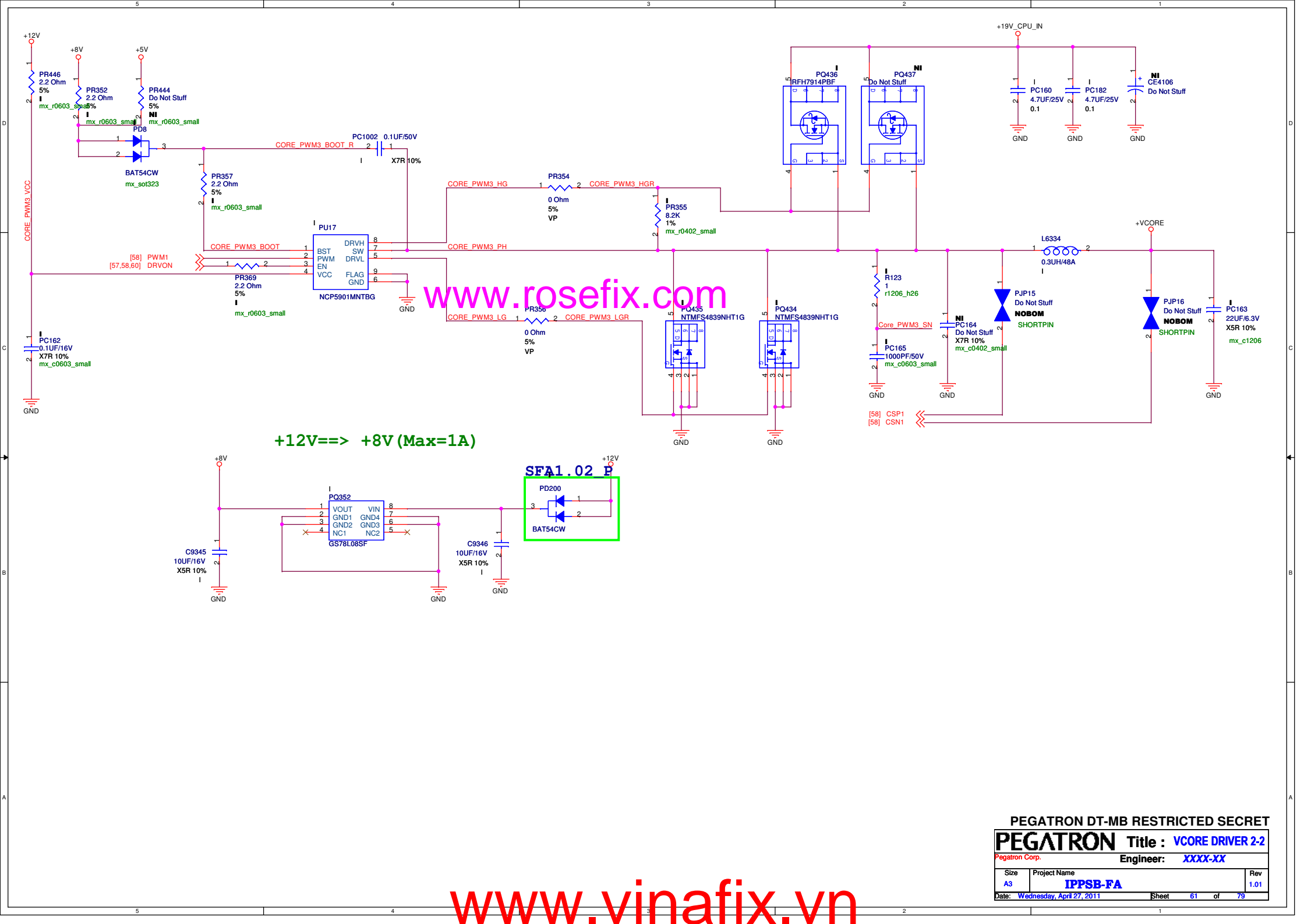
PL-CAP *4 +2(NI)
MLCC *18 +3(NI)

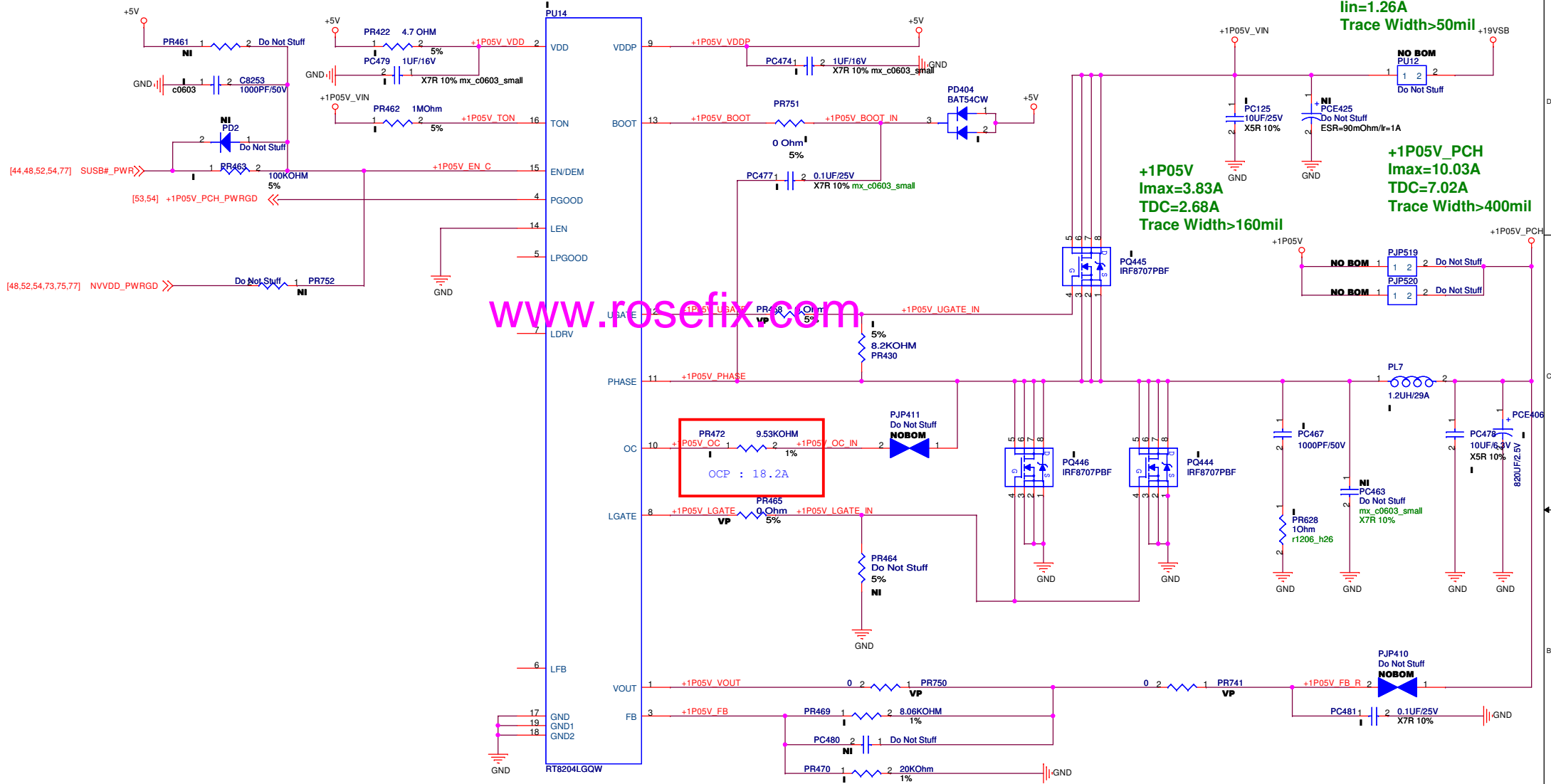


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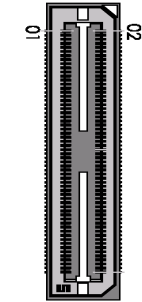
www.vinafix.vn



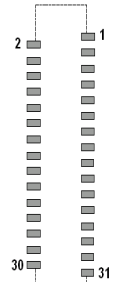




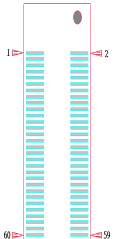
INTEL PCH XDP DEBUG PORT



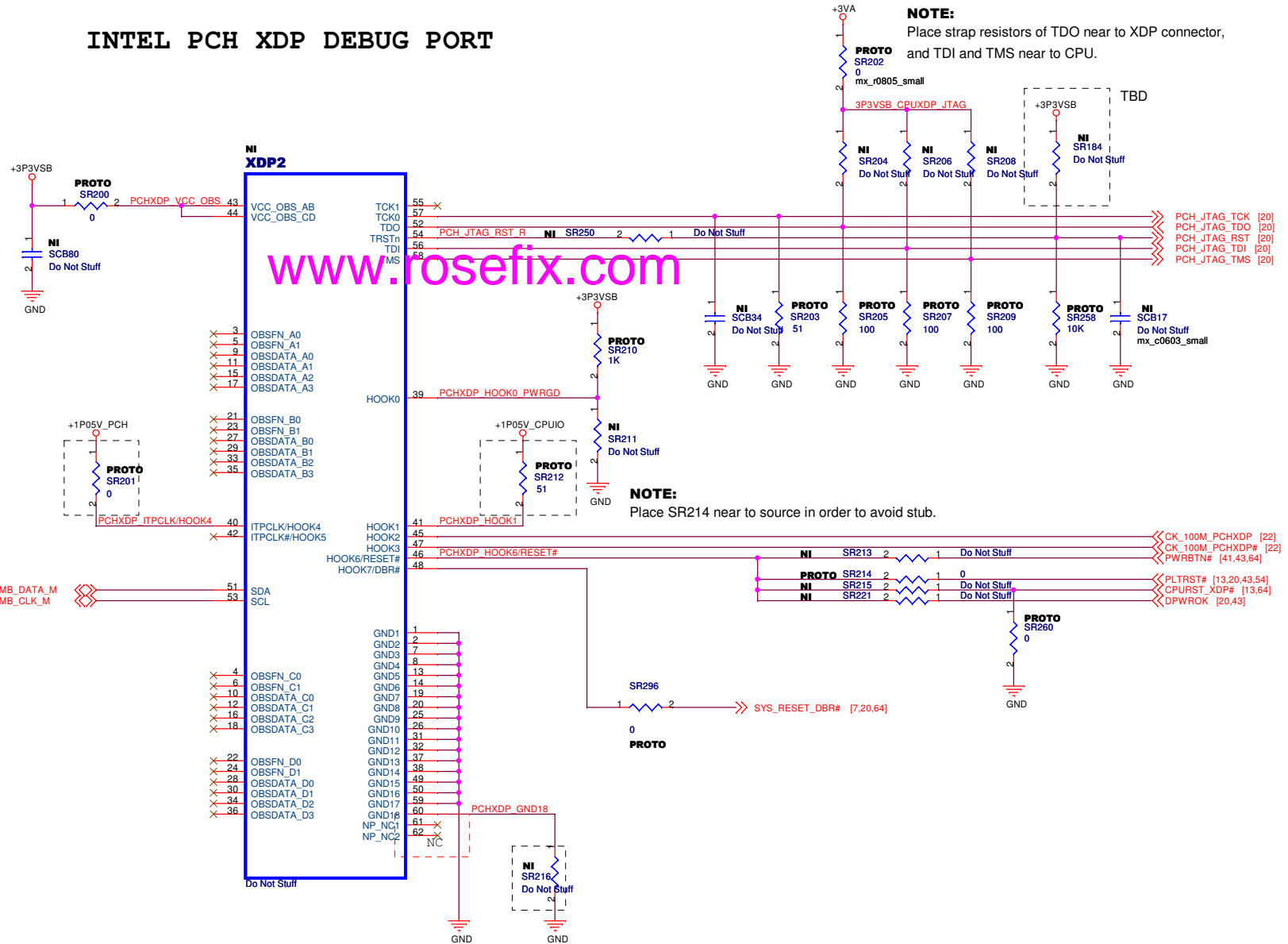
TOP SIDE VIEW

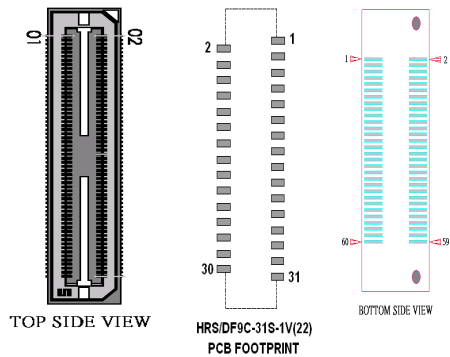


HRS/DF9C-31S-1V(22)
PCB FOOTPRINT

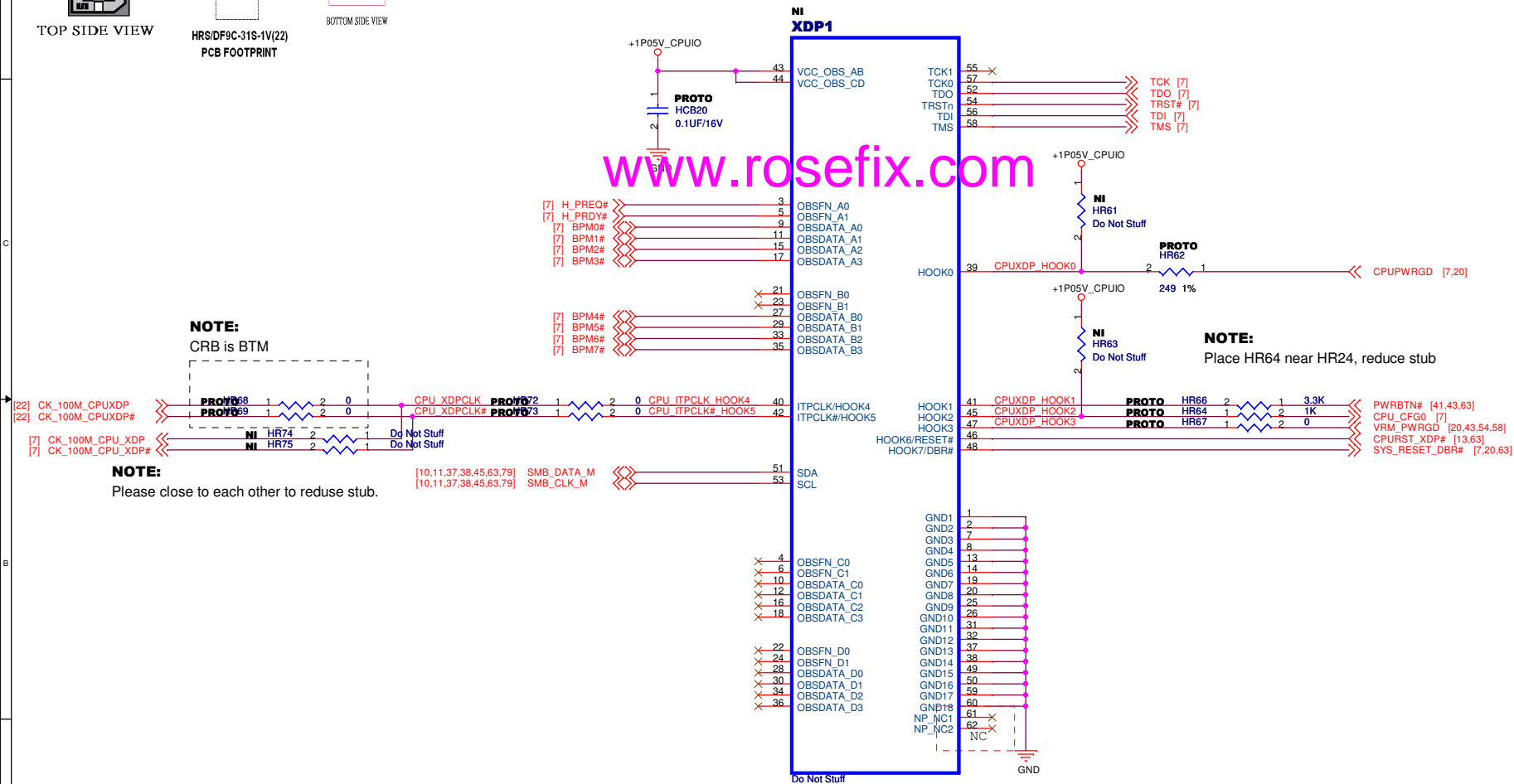


BOTTOM SIDE VIEW





INTEL CPU XDP DEBUG PORT



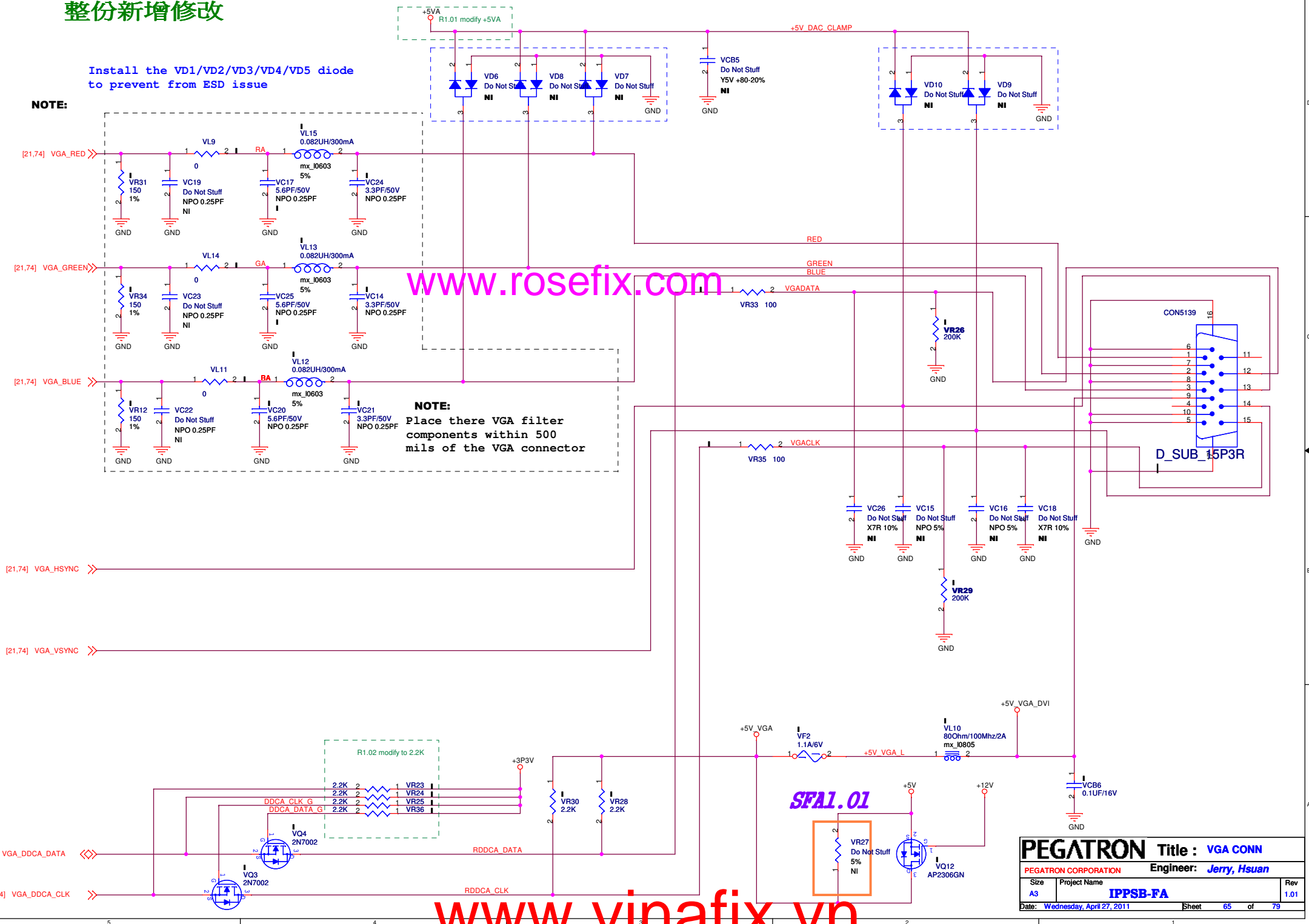
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : CPU XDP DEBUG	
PEGATRON CORPORATION		Engineer: XXXX-XX	
Size	Project Name	Rev	
A3	IPPSB-FA	1.01	
Date: Wednesday, April 27, 2011	Sheet	64	of 79

整份新增修改

Install the VD1/VD2/VD3/VD4/VD5 diode to prevent from ESD issue

NOTE:



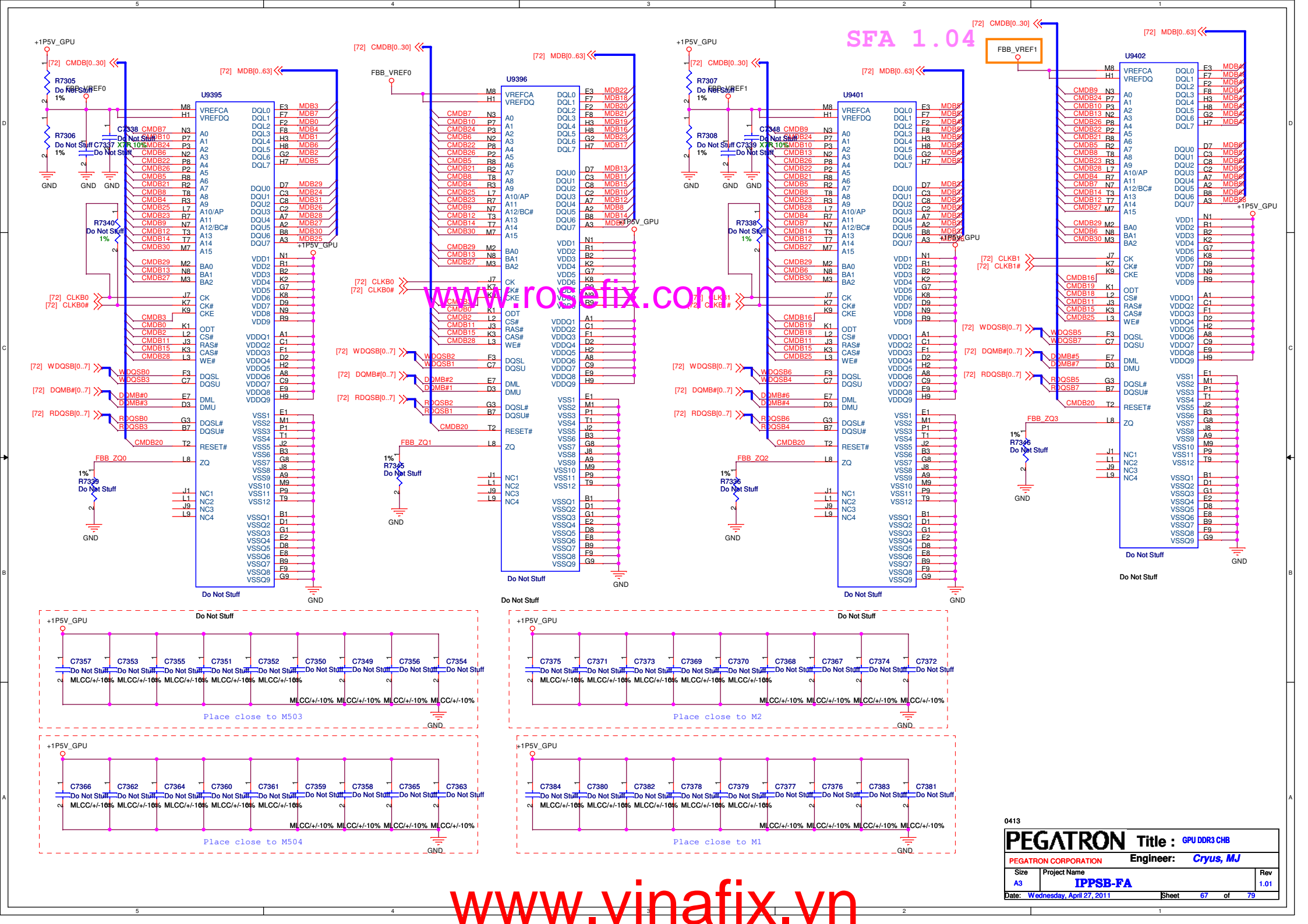
www.rosefix.com

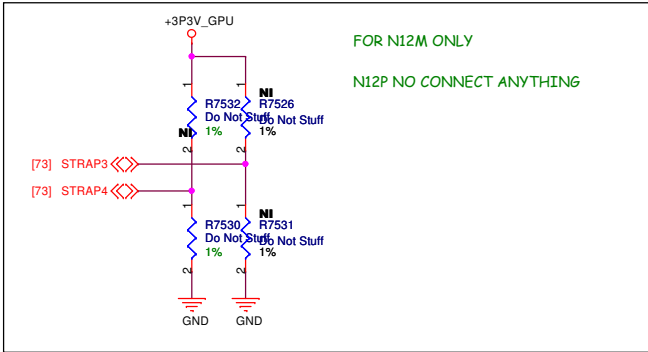
NOTE:
Place there VGA filter
components within 500
mils of the VGA connector

SFA1.01

PEGATRON		Title : VGA CONN	
PEGATRON CORPORATION		Engineer: Jerry, Hsuan	
Size A3	Project Name IPPSB-FA	Rev 1.01	
Date: Wednesday, April 27, 2011		Sheet 65 of 79	

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ROM_SI	bit0	RAM_CFG_0	1Gb (64Mx16 8pcs)
	bit1	RAM_CFG_1	RAM_CFG[3:0] Definitions
	bit2	RAM_CFG_2	0x2: Hynix => H5TQ1G63BFR-12C
	bit3	RAM_CFG_3	0x3: Samsung => K4W1G1646E-HC12
	0x0010 : 15K PD		

ROM_SO	bit0	VGA_DEVICE	1: VGA Device (default class code 300h)
	bit1	SMB_ALT_ADDR	0: 0x9E (default)
	bit2	FB_0_BAR_SIZE	0: 256MB (default)
	bit3	XCLK_417	0: 277M Hz (default)
		N12P-6E 0x0001 : 10K PD	N12M-6S 0x1001 : 10K PU

different

ROM_SCLK	bit0	PEX_PLL_EN_TERM	0: Disable (default)
	bit1	SLOT_CLK_CONFIG	0: GPU & MCH not share common reference clock
	bit2	SUB_VENDER	0: no vidio BIOS ROM
	bit3	PCI_DEVID_4	1: PCI_DeVID[4] => 0x0DFE bit 4 = 1

N12P-6E 0x1100 : 35K PU

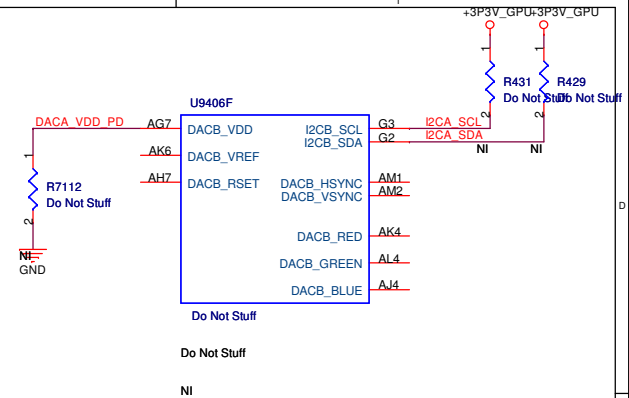
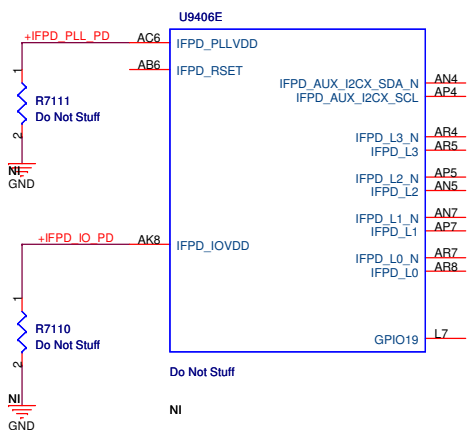
N12M-6S 0x1100 : 25K PU

different

STRAPO	bit0	USER_BIT0	0x0000 : 5K PD (Panels select Default 0x0000)
	bit1	USER_BIT1	
	bit2	USER_BIT2	
	bit3	USER_BIT3	

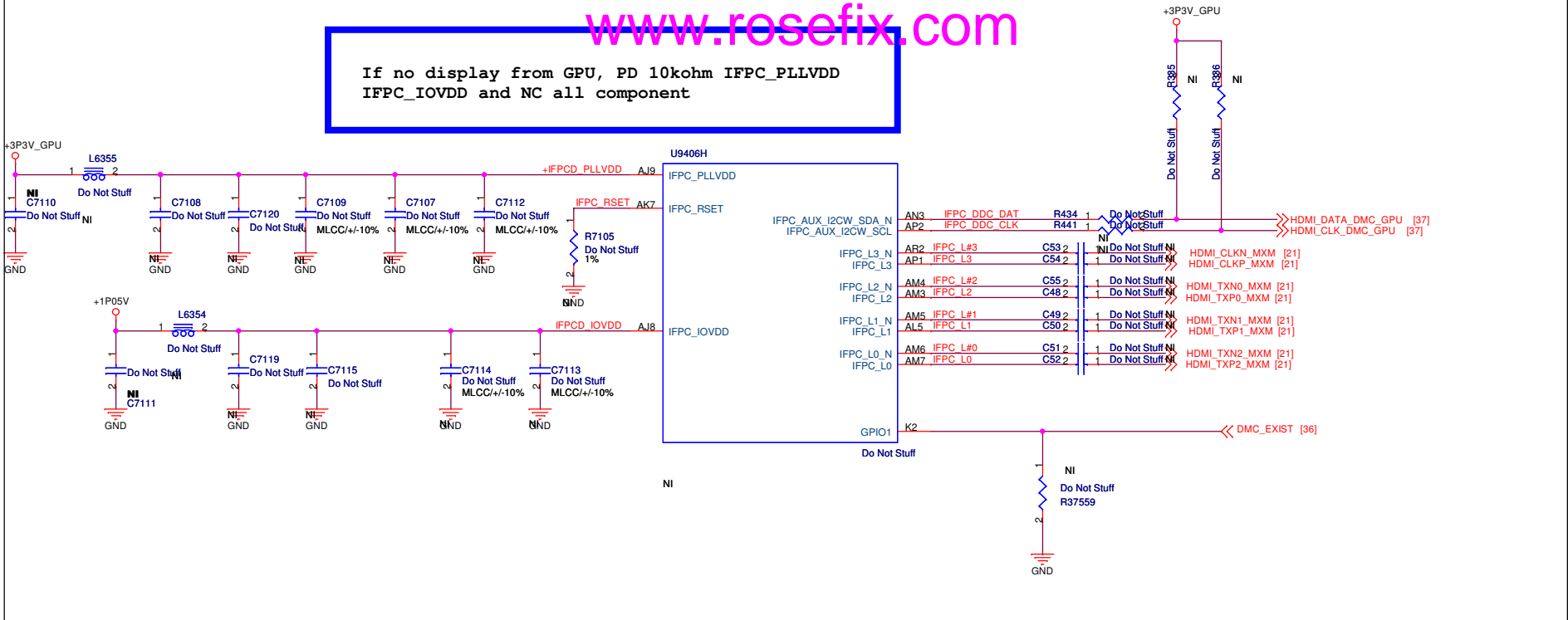
STRAP1	bit0	3GIO_PADCFG_LUT_ADRO	0x6 : 35k PD (PCIE swing default)
	bit1	3GIO_PADCFG_LUT_ADRI	
	bit2	3GIO_PADCFG_LUT_ADR2	
	bit3	3GIO_PADCFG_LUT_ADR3	

STRAP2	bit0	PCI_DEVID_0		
	bit1	PCI_DEVID_1		
	bit2	PCI_DEVID_2	N12P-6E 0x0101 : 30K PD	N12M-6S 0x0100 : 30K PD
	bit3	PCI_DEVID_3		

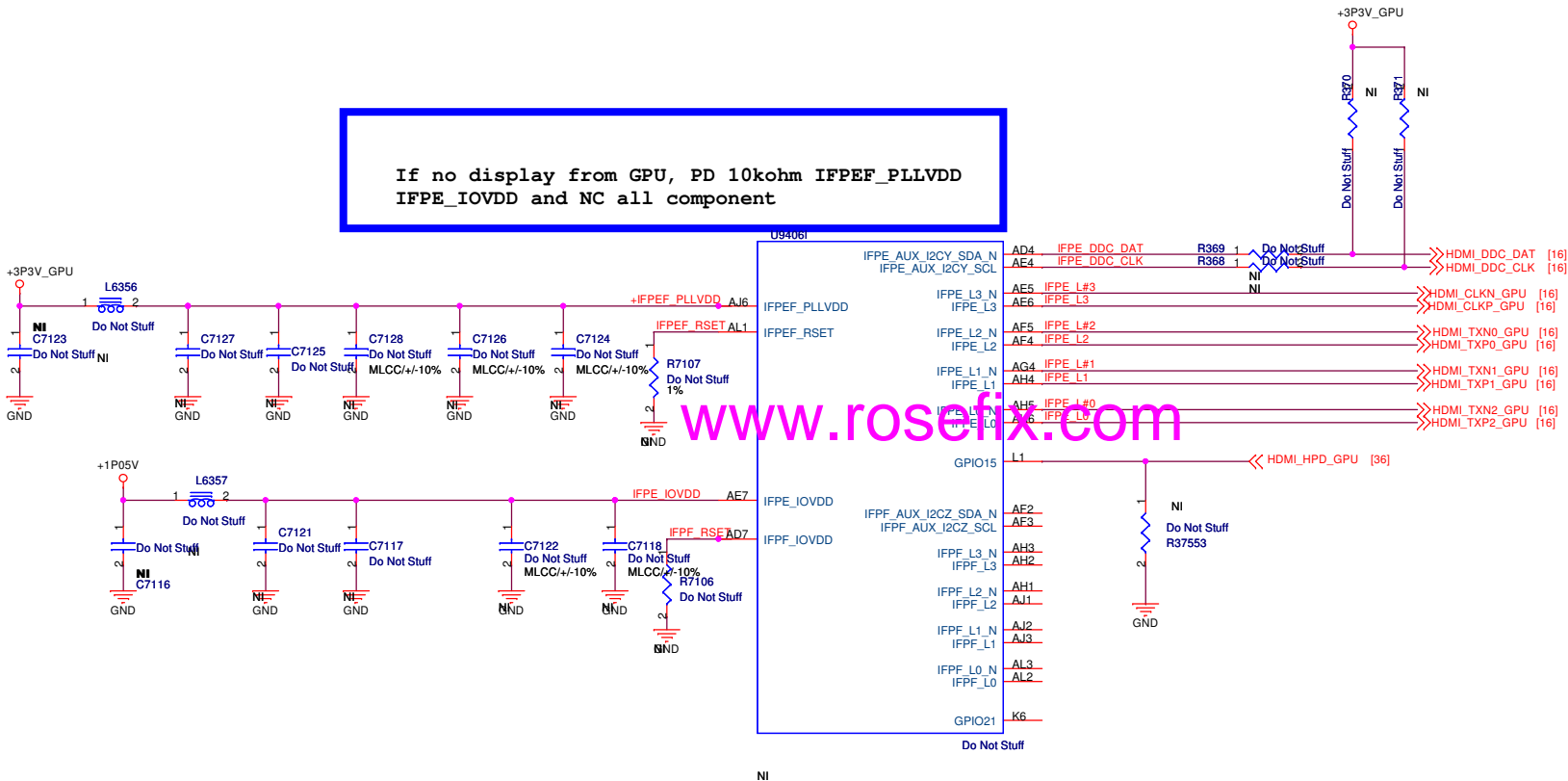


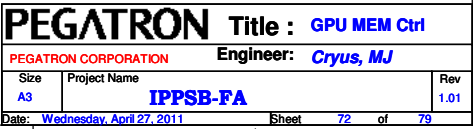
www.rosefix.com

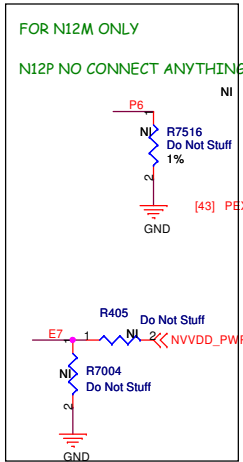
If no display from GPU, PD 10kohm IFPC_PLLVDD
IFPC_IOVDD and NC all component



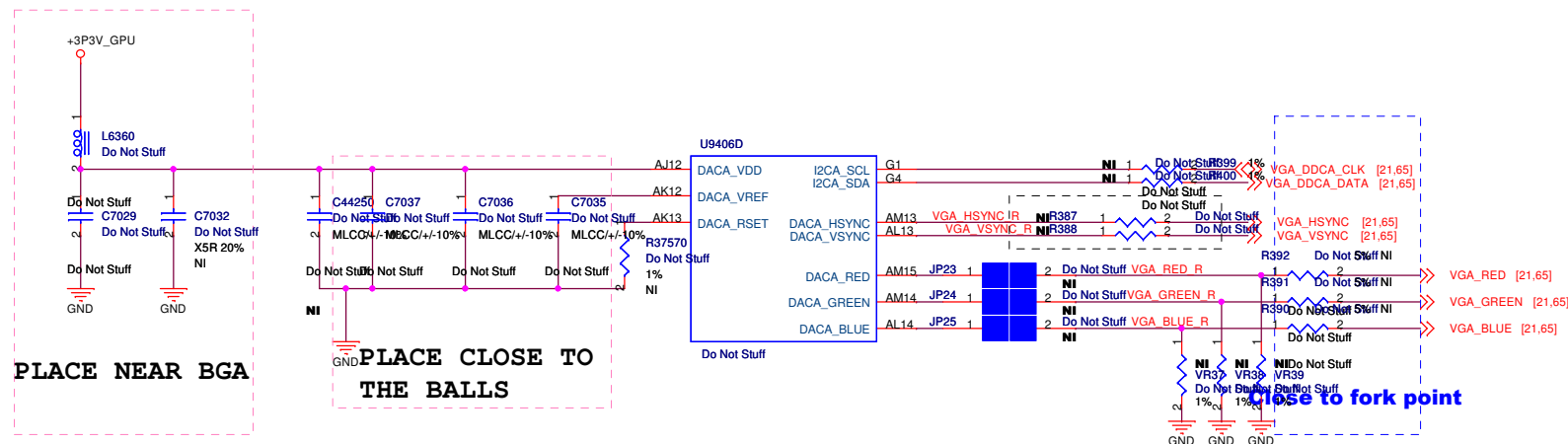
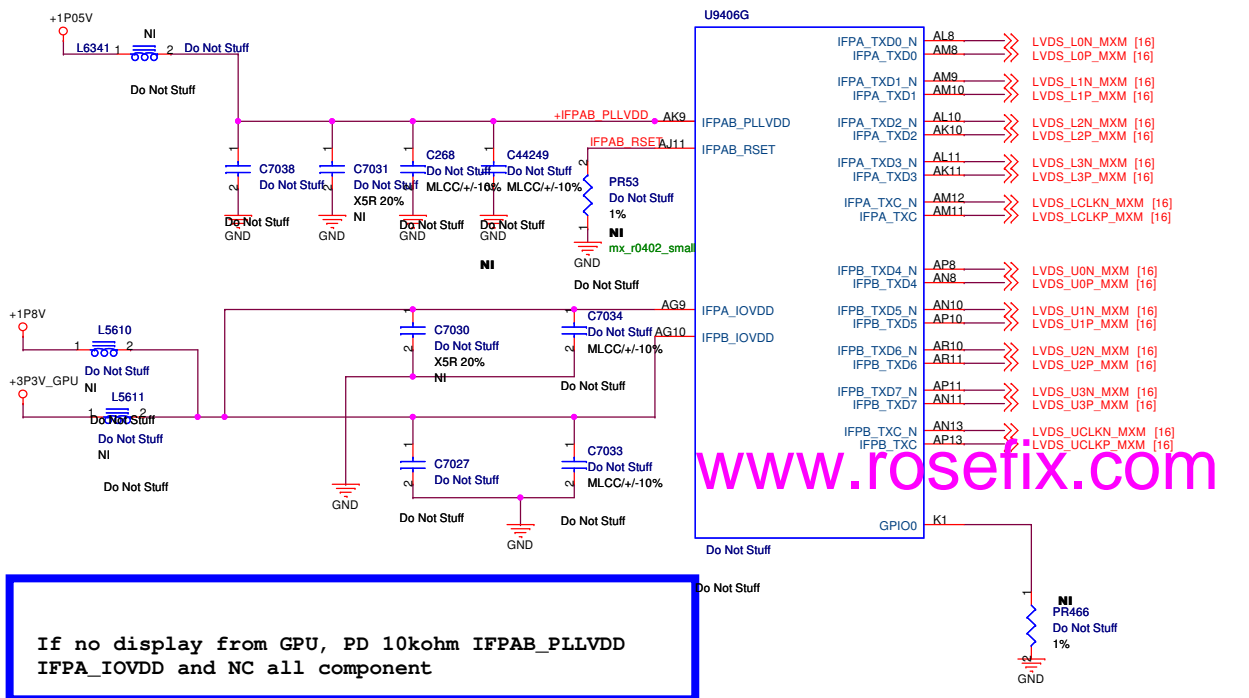
If no display from GPU, PD 10kohm IFPEF_PLLVDD
IFPE_IOVDD and NC all component







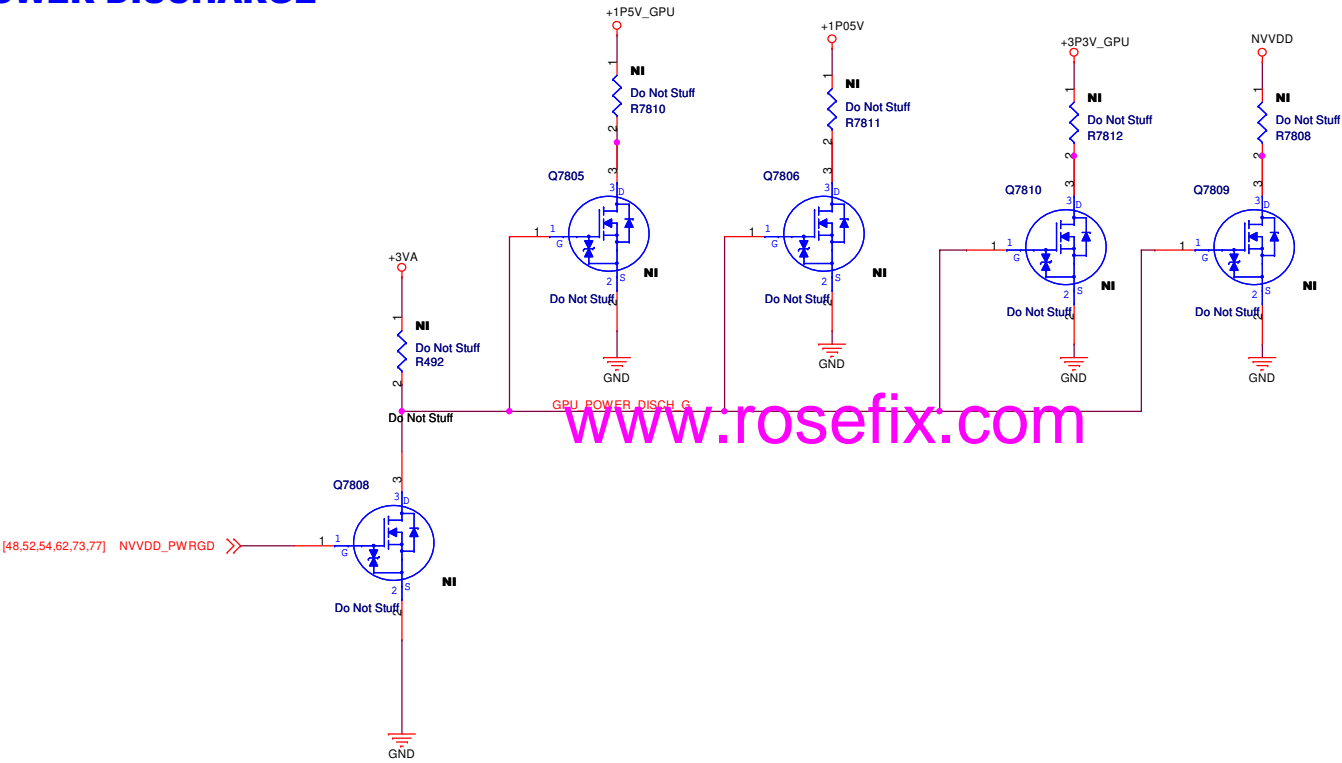
PEGATRON		Title : GPU PCI-E	
PEGATRON CORPORATION		Engineer: <i>Cryus, MJ</i>	
Size A3	Project Name IPPSB-FA	Rev 1.01	
Date: Wednesday, April 27, 2011	Sheet	73	of 79



0413

PEGATRON		Title : GPU LVDS VGA	
PEGATRON CORPORATION		Engineer: Cryus, MJ	
Size A3	Project Name IPPSB-FA	Rev 1.01	
Date: Wednesday, April 27, 2011		Sheet	74 of 79

GPU POWER DISCHARGE



0413

PEGATRON		Title : GPU Discharge	
PEGATRON CORPORATION		Engineer: Cryus, MJ	
Size	Project Name		Rev
A3	IPPSB-FA		1.01
Date: Wednesday, April 27, 2011		Sheet	75 of 79

12/28 新增
01/07 修改

